*Proceedings of the World Congress on Electrical Engineering and Computer Systems and Science (EECSS 2015)*
*Barcelona, Spain, July 13-14, 2015*
*Paper No. 153*

# Low Noise Dual Gate Enhancement Mode MOSFET with Quantum Valve in the Channel

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***Abstract***- A proposed Si-based series multi-gate E-MOSFET is discussed in terms of its design, static and dynamic transport properties and noise figure. In its simplest realization, the design involves two gates in series comprising an extra n(p)-doped junction in the p(n)-channel. The role of the nano-scale junction is twofold: to minimize the Miller effect in the enhancement mode to improve the frequency response and to create a quantum well to quench the current noise associated with the carrier velocity fluctuations. While dual-gate depletion structure results in a reduced carrier transition time along the entire channel path, the quantization effects serve as a current noise filter. Similar quantum valve can be realized in the form of a well both in n- and p-channel enhancement mode FET, whereas the majority carriers experience a tunneling through a similar shape barrier. Doping concentration and size of the middle junction are free parameters and can be adjusted to the required figures of merit. AC device simulations confirm the expectations based on the along-the-channel potential profile: enhanced cutoff frequency and higher saturation current are the signatures of the reduced transition and RC-time, whereas the minimum noise figure and transfer functions demonstrate noise filtering capabilities of the state quantization.

***Keywords:*** Enhancement mode MOSFET, Dual gate, Quantum valve, Noise

## 1 Introduction

A dual gate field-effect transistor (FET) has been demonstrated as having unique advantages as compared to traditional single-gate FET, the way the parallels can be made between tetrode and triode tubes [1]. The list of improvements includes a substantial Miller effect reduction, more options in terms of control of the driving field along the channel in order to minimize the effect of the carrier mobility roll-off, and higher leverage in signal modulation. While the tetrode configuration so far was considered in depleted mode type of FET, here the focus is on the enhancement mode FET, which is the common switching element in CMOS technology. Particular interest is on the use of the middle junction which may serve not only as a restoration element for the enhanced channel but also as a quantum valve bandpass filter if designed properly. That the multi-gate or distributed gate FET design offers additional options in tailoring field along the channel and thus in performance improvement, is well established and is the essence of the FinFET technology (see e.g. [2] and references therein). The idea of the tailoring field was considered earlier in conjunction with the studies of 2DEG in MOSFET and HEMT technology [3, 4]. It was demonstrated that a FinFET with two wrapped gates biased in a certain way provides a uniform transconductance vs. gate bias alterations as compared to a conventional FinFET [5], although with somewhat reduced magnitude of the gain.

Our study shows that introduction of a serial multi-gate structure in enhanced mode MOSFET design offers not only better control of the field and thus a uniform transconductance, higher gain and enhanced breakdown voltage, but also substantially increased cutoff frequency and reduced level of noise due to em-

bedded extra junction in the channel. Results of device simulations taking into account filtering states caused by presence of the junction-related quantum well are reported and discussed in Sections 2, 3.

## 2 A proto-type dual gate E-MOSFET: design and I-V characteristics

The device structure and band diagrams are illustrated in Fig. 1 for a proto-type single gate NFET and Fig. 2 for a proto-type dual gate enhancement mode MOSFET (E-MOSFET), the latter has an embedded middle junction with doping level $5 \times 10^{20}$ cm$^{-3}$ and the width of 50 nm. At the current doping map, the threshold voltage $V_{TH}$ is about 0.8 V in all cases. Numerical analysis is performed using ATLAS simulator [6]. No actual optimization of the device parameters have been done this time, that is why the results discussed here refer to a proto-type design to illustrate the major trends in the DC and AC performance, with the single gate FET used as a reference system.

As easily seen on the I-V curves, Fig. 3, there is a noticable effect of the middle junction on the magnitude of saturation current, if both gates are kept at the same DC bias, the gate bias $V_G$ ramped up from 1.0 V to 2.6 V with a step of 0.4 V. The transconductance $g_m$ shows similar trends growing from 2.8 to 3.5 $\mu A/V$ linearly with the gate bias in case of the dual gate and from 2.8 to 3.25 $\mu A/V$ in the reference system. However, saturation current is systematically higher in the dual gate design, - an effect of more distributed double depletion region upon the potential profile, causing the driving field to ramp up twice - before the middle junction and then again gaining as approaching the drain after it drops to the initial value in the region of the quantum valve junction. Higher, by 6%, transconductance and higher, by 15%, saturation current of the split gate FET can qualitatively be interpreted in terms of the ratio between (dual gate)-(single gate) transit times. The ratio can be estimated as

$$\frac{\tau_{dg}}{\tau_{sg}} \sim \frac{\sum_{i=1}^{2} \cosh^{-1}(1+n_{i,sg})\sqrt{1/n_{i,sg}}}{\sum_{i=1}^{2} \cosh^{-1}(1+n_{i,dg})\sqrt{1/n_{i,dg}}},$$

where $n_i$ stand for the slope of the field, $i = 1,2$ labels the halves of the channel. The double-depletion structure of the dual gate leads to a situation when there is also two regions of the field build-up: from source edge to the first wall of the QW, and from the second wall of the QW to the edge of the drain. The highly doped region of the QW sets a nearly constant potential and thus results in vanishing the field in the QW region. Given the field profile, the ratio turns to be $\sim 0.85$, which explains the I-V trends discussed.

The Early voltage is practically immune to the drain and the gate bias in both designs.

Due to a considerable Miller effect reduction, the frequency response has a significant improvement due to the middle junction, raising transition frequency from $f_T = 30$ GHz in case of a single gate FET to $f_T = 90$ GHz for the dual gate FET, even for that un-optimized version of the device. Within the indicated frequency range, the simulated overlap capacitance $C_{GD}$ is estimated at 0.075 fF/$\mu$ for the dual gate design, which is a factor of 4 less than 0.3 fF/$\mu$ for the reference FET. The cutoff frequency stays practically unchanged for various size of the quantum valve, from a relatively large 100 nm, which mounts to about 3.3% of the total channel length L, down to 5 nm,- just 0.16% of L. Dimensions of the individual gates and the space between them seem to play a dominant role in shaping the frequency response of the AC characteristics such as voltage gain and the network S-parameters, emphasizing the reduced capacitive effect as primary reason for the enhanced transition frequency

## 3 Quantum valve as a Bandpass filter: Noise reduction

Results of small-signal AC noise simulations are derived using the method of local current injection and its voltage response with subsequent integration over the entire device. It is assumed that the noise from one point in the device is totally uncorrelated with the statistical behavior of the noise at other points. Currently,

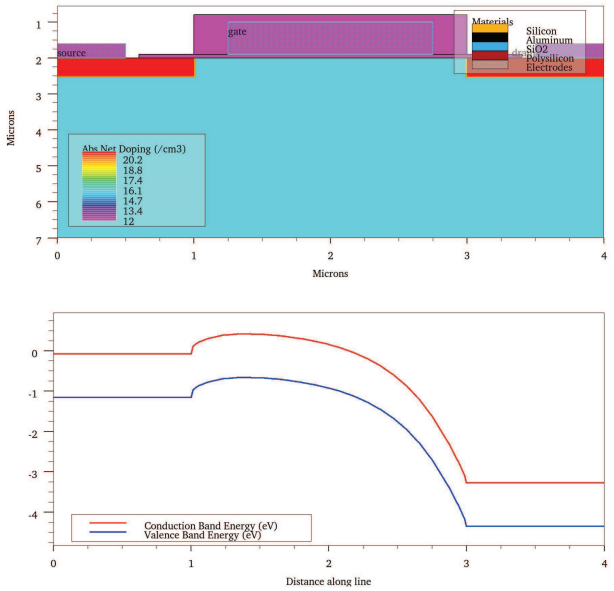


Fig. 1: Design and band structure of the valence and conduction states, single gate proto-type NFET.

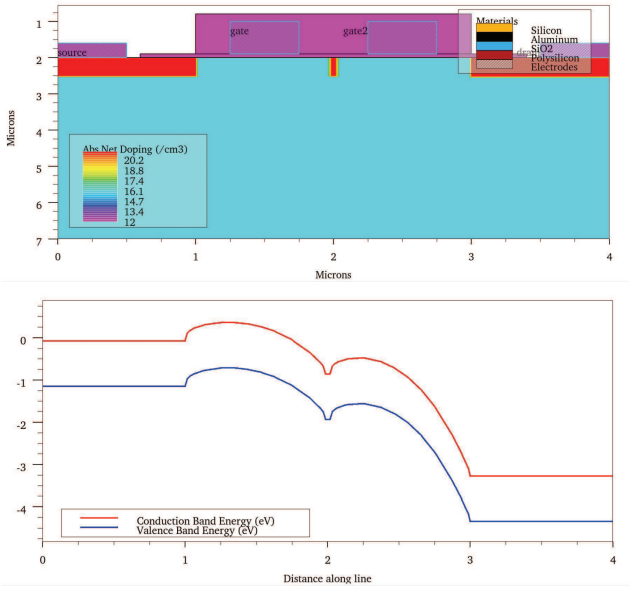


Fig. 2: Design and band structure of the valence and conduction states, dual gate proto-type NFET, middle junction-associated QW width is 50 nm.

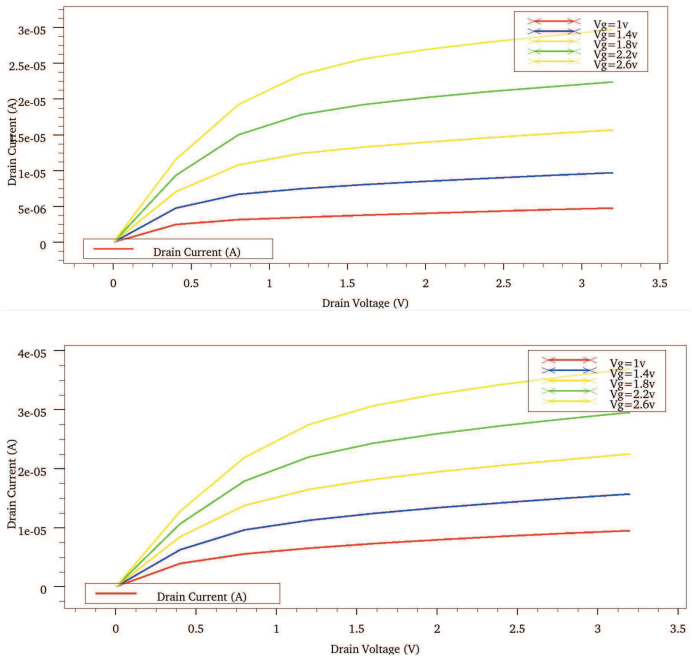


Fig. 3: I-V characteristics, single (top) and dual gate (bottom) proto-type NFET, middle junction-associated QW width is 50 nm.

the variations of the carrier velocity by diffusing from the injection spot to the open circuit contact serve as a source of the noise.

It is well known that a quantum well may serve as an efficient bandpass filter if the carrier energies are close to the confined levels, - an idea formally based on the fact that the thermal noise power scales linearly with the temperature, resistance and the bandwidth. Similar effects are well known in resonant tunneling devices based on the alternating barrier/well layered structures, which can be described in terms of a matrix element coupling the current fluctuation at a longitudinal energy with the transmission probability fluctuation at another energy, as shown e.g. in [7, 8, 9]. In case of an individual QW representing a dual function middle junction, the quantized subbands serve as a pool of carriers with reduced longitudinal fluctuations of current density to the right-hand side part of the channel. This may lead to a situation with reduced fluctuations of

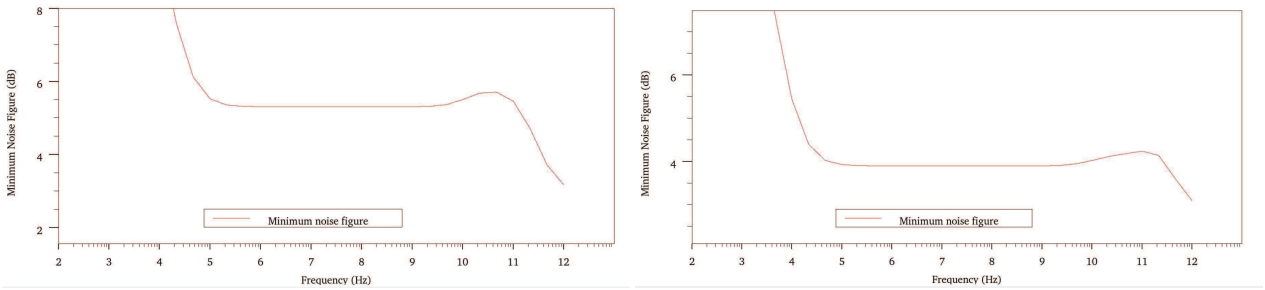


Fig. 4: Minimum noise figure, single gate FET (left) and dual gate FET (right) with 50 nm QW in the middle.

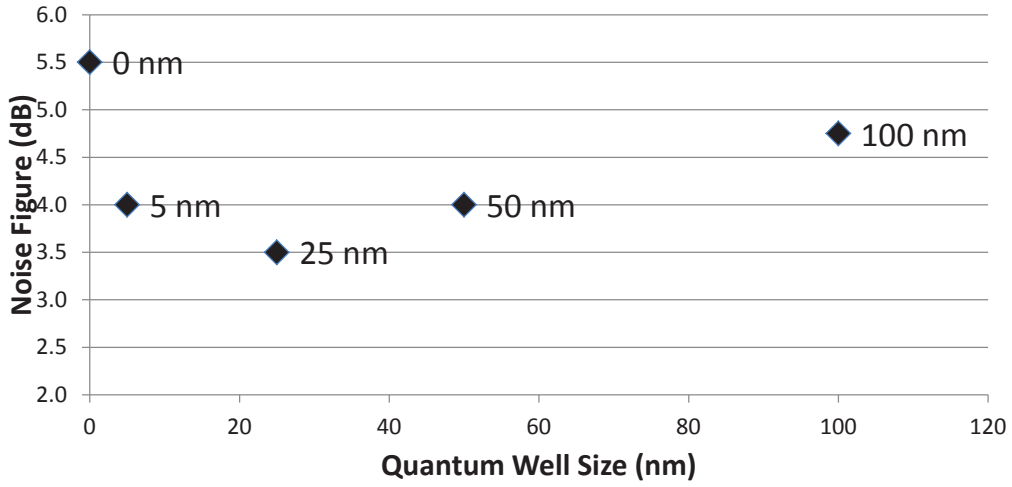


Fig. 5: Minimum noise figure versus QW size, data at 0 nm QW size describe the reference system.

current and voltage depending on the parameters of the QW and the bias across the channel. The important figure of merit here is the minimum noise figure defined as a log of ratio between SNR power at the input to that at the output of a device. According to Fig. 4, the noise figure is about 5.7 dB in a wide range of frequencies for the single gate FET, whereas it is by a significant 30% less in case of QW FET and mounts to 4 dB in the same frequency range, whereas the parameters of the QW is 50 nm in width and 0.35 eV in depth. Varying the QW size from 100 nm down to 5 nm while keeping same depth of 0.35 eV (controlled by the doping), the following trend is established: the noise figure drops from 5 dB at 100 nm QW, to 4 dB at 50 nm QW, further to 3.5 dB at 25 nm QW, and even at 5 nm QW it is still below 4.0 dB, as illustrated in Fig. 5.

The subband structure in the non-tilted, i.e. with no source-drain bias $V_{ds}$, well changes as following: 37 bound states at 50nm, 14 bound states at 25 nm and just 3 states at 5 nm QW. Applying $V_{ds}$ leads to a reduced number of quantized states in the tilted QW, which is statistically more essential at smaller well width. Although, the states at the top of the QW are more crucial due to their higher statistical weight in the integral expression for the current density, rendering the noise level highly sensitive in the range of smaller QW. Fewer quantized states filter out the current fluctuations more efficiently due to fewer number of the

momentum allowed in the well, thus rendering smaller valve size as more beneficial for the noise reduction. Obviously, the fluctuation quenching capability starts deteriorating as the density of subbands in the upper part of the well drops with the well width, and the noise returns back to the level of the reference device when the QW is narrow enough. At the DC bias at which the Fig. 5 is obtained, the return point for the noise is around 5 nm QW, when there is only one subband in the tilted QW located at the very top of the well. This conclusion offers also high promises for short channel FET devices, as it allows keeping the aspect ratio of the channel length to the QW width, LW, as high as possible in order to minimize the impurity scattering.

## 4 Conclusions

A concept of series dual-gate E-MOSFET is used to achieve a potential profile which involves an embedded quantum well in the inversion channel. In its simplest realization, the design involves two gates in series and additional highly-doped junction in between. The role of the nano-scale junction is twofold: to minimize the Miller effect in the enhancement mode to improve the frequency response and to create a quantum well to quench the current noise associated with the carrier velocity fluctuations. While dual-gate depletion design allows to effectively reduce the transition time along the entire channel path, the quantization effects serve as a current noise filter. Similar quantum valve effect involving minority carriers is present in both n- and p-channel FET, whereas majority carriers experience a tunneling through a mirror-image barrier. Doping concentration and size of the middle junction are free parameters and can be adjusted to the required figures of merit. AC device simulations confirm the expectations based on the along-the-channel potential profile: enhanced cutoff frequency and higher saturation current are the signatures of the enhanced mobility, whereas the minimum noise figure and transfer functions demonstrate noise quenching capabilities of the state quantization.

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