

A 12-bit CMOS Ratio-Independent Algorithmic Analog-to-Digital Converter

Chi-Chang Lu

Department of Electrical Engineering
National Formosa University
64, Wenhua Road, Huwei, Yunlin 632, Taiwan, R.O.C.
Email: cclu@nfu.edu.tw

Abstract -This paper proposes a 1.5 V 12-b CMOS ratio-independent algorithmic analog-to-digital converter (ADC) based on a capacitor-mismatch insensitive technique. A novel switched-capacitor multiplying digital-to-analog converter (MDAC) with an accurate gain of two is proposed for an algorithmic ADC. The proposed MDAC architecture requires only one opamp in four phases to generate the next residue output voltage. It significantly suppresses the gain error caused by a capacitor mismatch. Furthermore, bootstrapped switches are used to achieve rail-to-rail signal swing at low-voltage power supply. This ADC design achieves a DNL and INL of 0.36 LSB and 0.45 LSB, respectively, while the SNDR is 61.8 dB and SFDR is 69.5 dB at an input frequency of 400 kHz. Operating at a 5 MS/s sampling rate using a single 1.5 V power supply, the power consumption is 4.8 mW in a TSMC 0.18 μm CMOS 1P6M process.

1. Introduction

Because of the rapid development of digital signal processing, a signal can be processed conveniently and efficiently using digital processing. Consequently, the interface using an analog-to-digital converter (ADC) has become a central component and plays a vital role in system chip designs.

In recent years, system portability has become prevalent, thus increasing the demand for low-voltage and low-power circuits, such as circuits for bio-medical applications. In the algorithmic ADC, the residue voltage is cyclic, requiring only one stage. To meet the stringent requirements regarding chip area and power consumption, the algorithmic ADC is an attractive choice [1] [2] [3]. However, the gain error resulting from a capacitor mismatch is the main delimiter of achievable accuracy for the algorithmic ADC. In the relevant literature, various techniques have been developed to overcome the capacitor mismatch problem. However, the conventional ratio-independent algorithmic ADC requires two opamp and a comparator [1]. This paper proposes an algorithmic ADC that requires only one opamp in four phases to generate the next residue output voltage.

The remainder of this paper is organized as follows: Section II reviews the conventional algorithmic ADC architecture and discusses the sensitivity to a capacitor mismatch; the proposed capacitor-mismatch insensitive multiplying DAC is also presented; Section III details the implementation of the CMOS building blocks; simulation results are presented in Section IV; and Section V presents the conclusion.

2. Architecture Of The Proposed Algorithmic Adc

The algorithmic ADC is also known as the cyclic ADC. The block diagram of the conventional algorithmic ADC is shown in Fig. 1 [1]. The algorithmic ADC consists of a front-end S/H circuit, multiply-by-two amplifier, comparator, reference-subtraction circuit, and shift registers. For an N -bit conventional cyclic ADC, $N + 1$ cycles are required to complete an N -bit conversion.

In Fig. 1, the functions of the S/H circuit, multiply-by-two amplifier, and reference-subtraction circuit can be accomplished by a multiplying digital-to-analog converter (MDAC). In the design of an algorithmic ADC, the MDAC is the fundamental building block. Fig. 2 shows the conventional capacitor flip-over MDAC.

The circuit operates as follows: During the sampling phase, the input voltage is sampled on two identical capacitors, C_S and C_F . During the amplification phase, the capacitor C_F switches positions in the opamp feedback loop, while the capacitor C_S is switched to V_{ref} or 0, depending on the output of the comparator. A capacitor mismatch is assumed between C_S and C_F ; that is, $C_S = C$ and $C_F = C(1 + \varepsilon)$, where ε is the relative mismatch error.

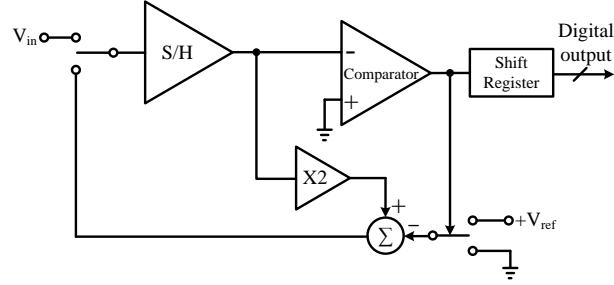


Fig. 1. Block diagram of the conventional algorithmic ADC.

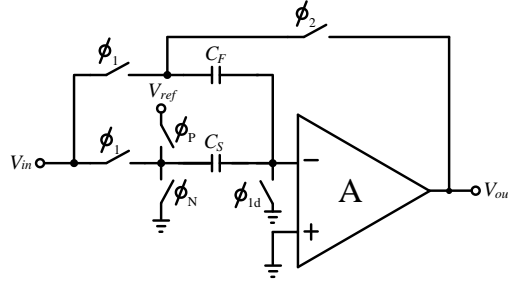


Fig. 2. Schematic of the conventional capacitor flip-over MDAC.

If the finite opamp gain error and offset are neglected, the output voltage would be

$$V_{out} = \left(2 - \frac{\varepsilon}{1 + \varepsilon}\right) V_{in} + \left(\frac{1}{1 + \varepsilon}\right) D V_{ref}, \quad (1)$$

where the value of D can be 0 or 1.

In the ideal instance, the stage gain would be two; however, in practice, it is lower or higher than two. Therefore, a capacitor mismatch between C_S and C_F causes a nonlinear error and is the largest obstacle to realizing a high-resolution ADC. This problem can be solved by the ratio-independent technique. The design in [1] employs two opamp to accomplish residue sampling and multiplication function.

The architecture of the proposed algorithmic ADC, depicted in Fig. 3, consists of a Miller-capacitance-based S/H circuit, sub-ADC, and capacitor-mismatch insensitive MDAC. For simplicity, the single-ended schematic of the proposed capacitor-mismatch insensitive MDAC and four clock phases that drive the switches are shown in Fig. 4.

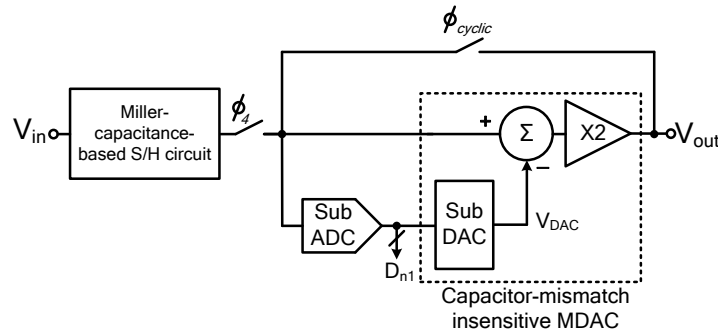


Fig. 3. Architecture of the proposed algorithmic MDAC.

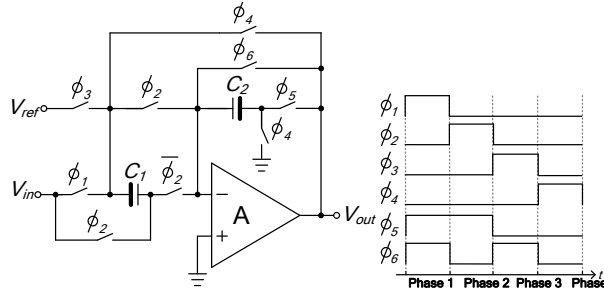


Fig. 4. Schematic of the proposed capacitor-mismatch insensitive MDAC.

The equivalent schematic circuit diagram of the proposed capacitor-mismatch insensitive MDAC in four clock phases is shown in Fig. 5. The circuit operates as follows:

During Phase 1, the input voltage V_{in} is sampled on the sampling capacitor C_1 . Simultaneously, the feedback capacitor C_2 is reset to be prepared for the next phase. The resulting charges stored on C_1 and C_2 are given by

$$Q_1(1) = C_1 \times V_{in} \quad (2)$$

$$Q_2(1) = 0, \quad (3)$$

where the parentheses and the subscript of Q represent the phase and the capacitor numbers.

During Phase 2, the MDAC is still in sampling mode; however, the plates of the sampling capacitor C_1 are interchanged. Because of charge conservation at the input node of the opamp, it follows that

$$Q_1(2) = C_1 \times V_{in} \quad (4)$$

$$Q_2(2) = -2C_1 \times V_{in} \quad (5)$$

During Phase 3, the input sampling capacitor C_1 may be connected to V_{ref+} or V_{ref-} , depending on the bit of the previous cycle. Simultaneously, C_2 is separated from the feedback loop of the opamp. At the end of this phase, the charge stored at C_2 is the same as that of Phase 2.

$$Q_1(3) = C_1 \times V_{ref} \quad (6)$$

$$Q_2(3) = Q_2(2) = -2C_1 \times V_{in} \quad (7)$$

During Phase 4, the charge stored at C_2 is dumped to C_1 . Therefore,

$$Q_2(4) = 0 \quad (8)$$

$$Q_1(4) = C_1 \times V_{ref} - 2C_1 \times V_{in} \quad (9)$$

From (8), the residue voltage at the opamp output is derived as follows

$$V_{out} = \frac{Q_1(4)}{C_1} = -2 \left(V_{in} - \frac{1}{2} V_{ref} \right) \quad (10)$$

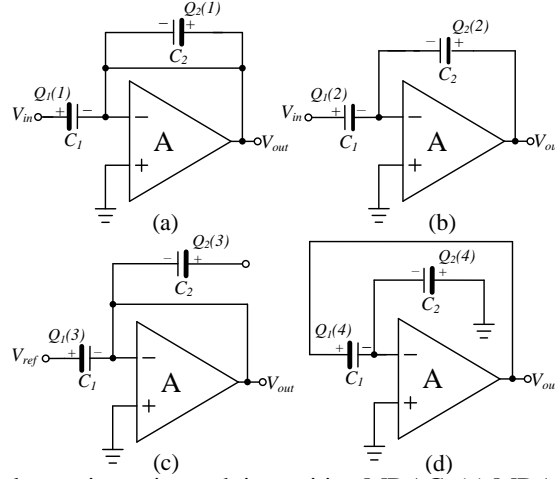


Fig. 5. The operation of the proposed capacitor-mismatch insensitive MDAC. (a) MDAC during phase 1. (b) MDAC during phase 2. (c) MDAC during phase 3. (d) MDAC during phase 4.

However, the actual implementation is fully differential and the polarity of the output voltage is resolved. The complete schematic is shown in Fig. 6.

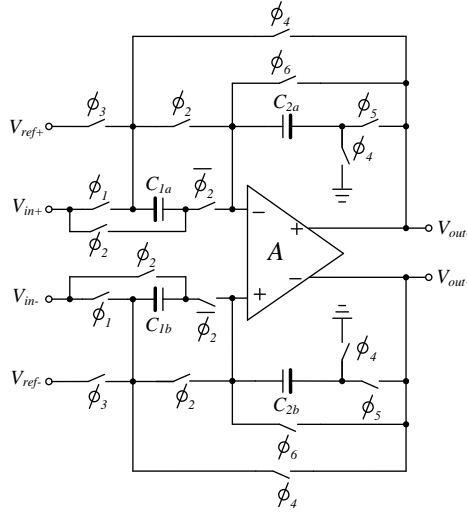


Fig. 6. The proposed fully differential capacitor-mismatch insensitive MDAC.

The differential residue voltage (V_{out+} , V_{out-}) at the opamp output is revised as follows

$$V_{out+} - V_{out-} = 2 \left[(V_{in+} - V_{in-}) - \frac{1}{2} (V_{ref+} - V_{ref-}) \right] \quad (11)$$

However, a fully differential structure results in a reduction of the common-mode hold pedestal and noise, as well as order distortion. The above equation shows that the exact gain of two is achieved because the amount of transferred charge is only associated with C_{1a} (C_{1b}) and because capacitor C_{2a} (C_{2b}) is only used as a temporary charge-storing element. In this scheme, the capacitor C_{1a} (C_{1b}) is the sampling capacitor during Phases 1, 2, and 3; however, it is employed as the feedback capacitor during Phase 4.

3. Circuit Description Of The Building Blocks

The basic building blocks of the proposed algorithmic ADC are described in this section.

A. Timing-skew-insensitive double-sampled Miller-capacitance-based S/H circuit

Compared with a conventional closed-loop S/H circuit, the Miller-capacitance-based S/H circuit [4] provides high-speed operation by using a low-signal-dependent hold pedestal, because the capacitor size is smaller and the

operational amplifier does not require slewing time. The single-ended schematic circuit of the timing-skew-insensitive double-sampled Miller-capacitance-based S/H circuit and its timing diagram are shown in Fig. 7. The actual implementation is fully differential. In the circuit presented in [4], the double-sampled architecture has two parallel signal paths, and a mismatch between them causes some errors degrading the circuit performance. There are three main sources of error in the double-sampled circuits: offset, a gain mismatch, and timing skew. However, the offset is not likely to be a problem because the opamp, which is the main source of offset, is common to both signal paths. A gain mismatch originating from a capacitor mismatch is a severe problem in some double-sampled circuits.

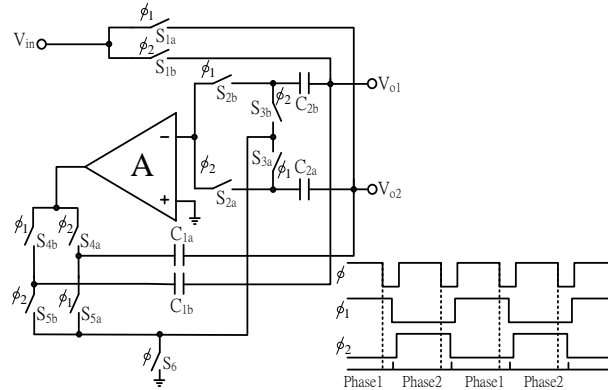


Fig. 7. Timing-skew-insensitive double-sampled Miller-capacitance-based S/H circuit and its timing diagram.

In the proposed scheme, the timing skew problem is overcome by a common sampling switch, which is controlled by a common clock signal to define the sampling instant. The circuit of Fig. 3 operates as follows:

During Phase 1, S_{1a} , S_{3a} , S_{5a} , and S_6 are on, while capacitors C_{1a} and C_{2a} sample the input signal. The total capacitance that must be charged or discharged is equal to $C_{1a} + C_{2a}$. Simultaneously, S_{2b} and S_{4b} are on, while C_{1b} , C_{2b} , and the opamp form a feedback amplifier. The effective hold capacitance is significantly increased by means of Miller feedback. Its value is typically much larger than the capacitance that must be charged during the sampling mode.

During Phase 2, the capacitor pairs are swapped: the input signal is sampled in capacitors C_{1b} and C_{2b} , while C_{1a} and C_{2a} are in the holding mode.

The common sampling switch S_6 , conducting during both phases, is controlled by a common clock signal ϕ and defines the sampling instant by applying a short zero pulse to switch S_6 , as shown in the timing diagram of Fig. 3. Clock signals ϕ_1 and ϕ_2 always go low after clock signal ϕ goes low. Even if there are large timing skews between successive clock signals ϕ_1 and ϕ_2 , they would not have any influence on the sampling instant; thus, the problem of timing skew is eliminated.

B. Bootstrapped switch

A major concern in designing ADC circuits on a low-supply voltage is the nonlinearity caused by the input sampling switches. Using an NMOS switch as a sampling switch in the proposed algorithmic ADC has two limitations: input-dependent ON-resistance and input-dependent charge injection. These limitations lead to nonlinear signal distortion. In this study, bootstrapped switches were employed to reduce this problem. However, because the bootstrapped switch circuit is complicated, it has been used in some critical places of the proposed ADC circuit. The other switches are NMOS devices.

Fig. 8 shows a bootstrapped switch circuit, which is a capacitance-level shifter [5]. Device M_9 operates as the sampling switch, turning on during phase $\phi_1(\phi_2)$ and off during $\bar{\phi}_1(\bar{\phi}_2)$. The bootstrapped switch circuit works as follows: when $\phi_1(\phi_2)$ is low, V_{DD} is applied across C_1 by M_3 and M_4 . Simultaneously, M_5 and M_6 are off, and the sampling switch M_9 is isolated. Node voltage V_G switches to ground to turn M_9 off. When $\phi_1(\phi_2)$ is high, M_5 and M_6 are on. The bottom plate of C_1 is connected to V_{in} , and then the voltage of the top plate is shifted to $V_{DD} +$

V_{in} . Node voltage V_G switches to $V_{DD} + V_{in}$ to turn M_9 on. The source voltage of M_9 is V_{in} ; thus, the V_{GS} of M_9 is V_{DD} , which is independent of V_{in} and larger than $V_{DD} - V_{in}$. Because the switch V_{GS} is relatively independent of signal, rail-to-rail signals can be used. The sampling switch linearity is improved, and the signal-dependent charge injection is also reduced.

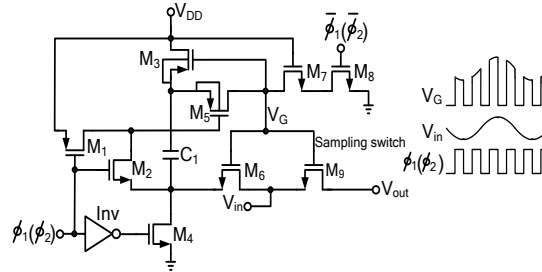


Fig. 8. Bootstrapped switch.

4. Simulation Results

The proposed low-voltage algorithmic ADC was designed using a 0.18 μm 1P6M CMOS technology and verified by Hspice and Matlab programs. Fig. 9 shows the layout of the ADC. Total layout area is approximately $1918 \times 1899 \mu\text{m}^2$. Fig. 10 shows the differential non-linearity (DNL) and integral non-linearity (INL), where the peak DNL is -0.25 – $+0.36$ LSB, and the peak INL is -0.45 – $+0.30$ LSB. Fig. 11 shows the spurious-free dynamic range (SFDR) and signal-to-noise-and-distortion ratio (SNDR) versus the input frequency at the conversion rate of 5 MHz. It exhibits the 12-b operation with an SFDR of 69.5 dB and SNDR of 61.8 dB at a 400 kHz input. It consumes 4.8 mW at a 1.5 V power supply.

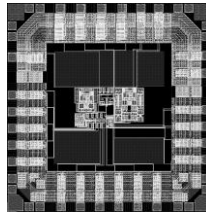


Fig. 9. Layout of the proposed algorithmic ADC.

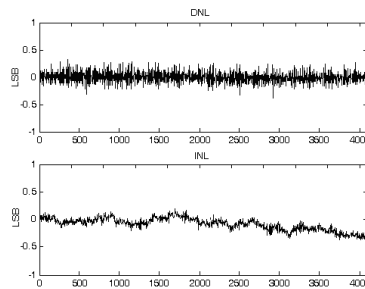


Fig. 10. Simulated DNL and INL versus output code.

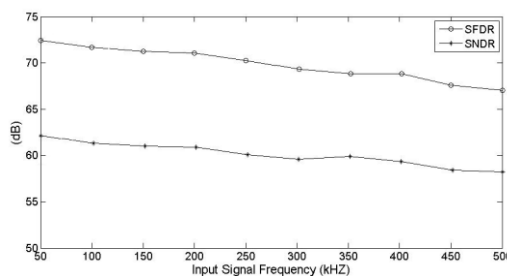


Fig. 11. Simulated SFDR and SNDR versus input signal frequency at 5 MS/s sampling rate

The performance of the proposed ADC is summarized in Table 1.

Table. I Summarized performance of the proposed ADC

Technology	TSMC 0.18 μ m 1P6M
Resolution	12-bits
Power Supply	1.5V
Conversion Rate	5 MSamples/s
Input Range	$\pm 0.5V$
DNL	-0.25 LSB ~ +0.36 LSB
INL	-0.45 LSB ~ +0.30 LSB
SNDR(@ f_{in} =400kHz)	61.8dB
SFDR(@ f_{in} =400kHz)	69.5dB
Power Dissipation	4.8mW

5. Conclusion

This paper presents a 1.5 V 12-b 5-MS/s CMOS algorithmic ADC with a capacitor-mismatch insensitive technique has been presented. Compared with conventional architectures, the mismatch between the capacitors has a considerably smaller influence on the accuracy of the gain of two. Simulation results demonstrate that the proposed ADC circuit is suitable for single-chip integration with recent low-voltage and medium-speed applications.

Acknowledgments

This work was supported by the National Science Council, Taiwan, Republic of China, under contract no. NSC 103-2221-E-150-064.

References

- Li, P. W., Chin, M. J., Gray, P. R., & Castello, R. (1984). A Ratio-Independent Algorithmic Analog-To-Digital Conversion Technique. *IEEE Journal of Solid-State Circuits*, 19(6), 828-836.
- Hatanaka, S., & Taniguchi, K. (2001). A Ratio-Independent Algorithmic Pipeline Analog-To-Digital Converter. *The 8th IEEE International Conference on Electronics, Circuits and System (ICECS)*, 1, 345-348.
- Jarvinen, J. A. M., Saukoski, M., & Halonen, K. (2007). A 12-Bit Ratio-Independent Algorithmic ADC For A Capacitive Sensor Interface. *Proceedings of the IEEE International Symposium on Circuits and Systems ISCAS'07*, 1713-1716.
- Lee, T.-S., & Lu, C.-C. (2005) A 1.5V 50mhz Pseudo-Differential CMOS Sample-And-Hold Circuit With Low Hold Pedestal. *IEEE Trans. Circuits and Systems-I*, 52(9), 1752-1757.
- Waltari, M., & Halonen, K. (2002). Bootstrapped Switch Without Bulk Effect In Standard CMOS Technology. *Electron. Lett.*, 38(12), 555-557.