Proceedings of the 2nd World Congress on Electrical Engineering and Computer Systems and Science (EECSS'16)
Budapest, Hungary – August 16 – 17, 2016
Paper No. EEE 112
DOI: 10.11159/eee16.112

An Area-Compact and High Power-Efficient Digital Buck Converter Using Nest-Loop Topology in 0.18um CMOS

Van Ha Nguyen, Jinwoong Choi, Ala'aDdin Al Shidaifat, Myeong-geun Kim, Keun Yong Sohn, Hanjung Song
Inje University, Department of Nanosience and Engineering,
197 Inje-ro, Gimhae, Republic of Korea
nguyenha@oasis.inje.ac.kr; hjsong@inje.ac.kr

Extended Abstract

Due to the mature of fabrication technologies which results in a scaling down of the power supply as well as the need of expanding working time of battery-powered portable devices, digital dc-dc buck converters have been considered as an excellent solution for replacing conventional dc-dc buck converters using analog control method. This is mainly because of the digital dc-dc converter: (1) can operate under a much lower voltage, (2) does not have static power since it eliminates all analog parts like an amplifier and comparator; therefore, the power efficiency in the digital buck converters is more attractive. In the literature, several buck converters have been designed with digital control methods using analog-to-digital converters (ADC); however, this scheme is not suitable for ultra-low-power applications because of its high power consumption as well as large chip area [1]. Recently, fully digital-based switching controllers have been developed [2,3]. These design can achieve very high power efficiency but also own several shortcomings such as high output voltage ripple. Although increasing the number of phase can further improve the resolution of digital PWM as well as the output voltage ripple, but it also increases the leakage and switching power of DFFs in the digital PWM controller [3]. In this paper a digital dc-dc buck converter with a novel nest-loop topology-based digital controller is proposed for low power applications. The proposed design consists of a clock generator, a nest-loop based digital PWM controller, and a power stage. The core of the design is the digital pulse width modulation (PWM) controller using a novel nest-loop topology that efficiently connects delay lines. By using the proposed scheme, high performance can be easily achieved in terms of resolution, output voltage ripple, power efficiency and number of used DFFs the without increasing number of phase as reported in [3]. The proposed design was simulated using a 0.18-µm CMOS process in order to verify the performance. The gained simulation results showed a very low power consumption of 1.16 µW at V_{DD} = 1 V and achieved a peak efficiency of 92.6% with a load current range of 3 mA to 10 mA with the number of used CMOS transistors were 2,194. Compared to the conventional design [3] simulated in the same condition, the proposed design reduced 58.4% of CMOS transistors, 58% of power consumption of the digital controller, and 49% of the output ripple of dc-dc buck converter. The low load current range of the dc-dc converter and the low power consumption of the proposed double-chain digital PWM make it very attractive for ultra-low-power applications.

Acknowledgements

This research was supported by the Human Resource Training Program for Regional Innovation and Creativity through the Ministry of Education and National Research Foundation of Korea (NRF-2014H1C1A1066686). This research was also supported by Korea Electric Power Corporation through Korea Electrical Engineering & Science Research Institute (R15XA03-66).

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