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A 3-wire SPI Protocol Chip Design with Application-Specific Integrated Circuit (ASIC) and FPGA Verification

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Abstract **-** This paper presents a 3-wire SPI protocol chip design for application-specific integrated circuit (ASIC) and field-programmable gate array (FPGA). It is the first study to realize SPI protocol by VLSI and FPGA technique for testing and verifying SPI protocol. The FPGA device is used as master device to control the ASIC design which is be as slave device. Moreover, the functions of SPI protocol is successfully worked by testing with oscilloscope. The ASIC design of this work contained 5.1 K gate counts and consumed 19 mW by using a TSMC 0.18 μm CMOS process. This work develops advanced VLSI architecture with only four pads (including system clock in ASIC design).

Keywords**:** Communication protocols, CMOS digital integrated circuit, digital signal process, electronic device measurement, testing, filed-programmable gate array (FPGA) verification and very-large-scale integration (VLSI)

1. Introduction

With the rapid development of microelectronic device, wearable technology, and internet of things (IoT), the communication protocol become an important issue. The basic concepts of inter-integrated circuit (I^2C) and serial peripheral interface (SPI) was proposed in [1]. The I^2C and SPI protocol provide an excellent solution for communicating between master device and slave device in the micro controller and system on chip [2-4]. In addition, many effective test methodologies for microelectronic device have been introduce in [5-8]. The characteristic of integrated circuit (IC) can be verified completely according to the testing structure. Hence, this paper firstly realized a 3-wire SPI protocol in the very large-scale integration (VLSI) technique. It is suitable for hardware implementation in VLSI applications due to the low complexity, high performance and low cost.

2. Principle of SPI Protocol

Serial peripheral interface (SPI) is one of communication protocol between master and slave device. The master device can regarded as an embedded system, field-programmable gate array (FPGA) or microcontroller and slave device can regarded as integrated circuit, electronic device or wearable technology. Fig. 1 (a) shows the block diagram of 4-wire SPI protocol. It includes a master device and a slave device. The SPI interface consists of two control signal and two data signal, which are chip select (CS), serial clock (SCL), serial data input (SDI) and serial data output (SDO) respectively. In general, the direction of two control signal and serial data input (SDI) are sent by master device and receive by slave device, we called "master out slave in (MOSI)". Conversely, the direction of serial data output (SDO) are sent by slave device and received by master device, we called "master in slave out (MISO)". Although the 4-wire communication protocol simplifies the numerous transmission line whether in the procedure of writing data or reading data, the silicon cost and power consumption are the major burden in VLSI technology, such as the package size of IC and the quantity of pad. Therefore, to minimize of the silicon area and increase the performance of the SPI system for VLSI applications, Fig. 1 (b) shows the block diagram of 3-wire SPI protocol. The principle of 3-wire SPI protocol is similar with 4-wire type. Compare with traditional 4-wir SPI protocols, the data signal is designed in port-shared. The advantage of 3-wire merged serial data input (SDI) and serial data output (SDO) into one port which is bi-directional. It has ability to handle the functions of

writing data and reading data in the same port. Compare with Fig. 1 (a), 3-wire SPI protocol achieve cost-efficient and higher performance for VLSI applications.

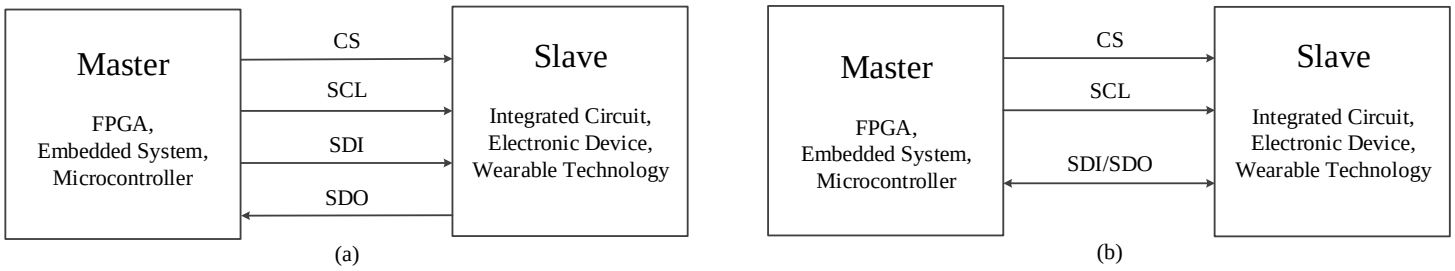


Fig. 1: Block diagram of (a) 4-wire SPI protocol (b) 3-wire SPI protocol.

The transmission waveform of 3-wire SPI protocol can be obtained by Fig. 2. The waveform design is ASIC and can be adaptively changed by the system designer. The master device sent logic "0" to the slave device by the CS port and the transmission will start. Otherwise, the transmission disabled. Fig. 2 (a) shows the waveform of 3-wire SPI protocol in procedure of writing data. Firstly, the CS convert into logic "0" and the SCL will provide a reference clock for SPI protocol. The total length of serial clock is 20 and the data signal will be setup and well prepared at positive edge of serial clock by the master device. In the same clock cycle, the data will be received to the slave device at negative edge of serial clock. The transmission serial data includes instruction, address, write data and "do not care" and the data width are 2, 8 (1byte), 8 (1byte), 2 bits respectively. Finally, the transmission finished after twenty serial clocks. By using the procedure of writing data, the slave device can acquired the new parameter from the master device.

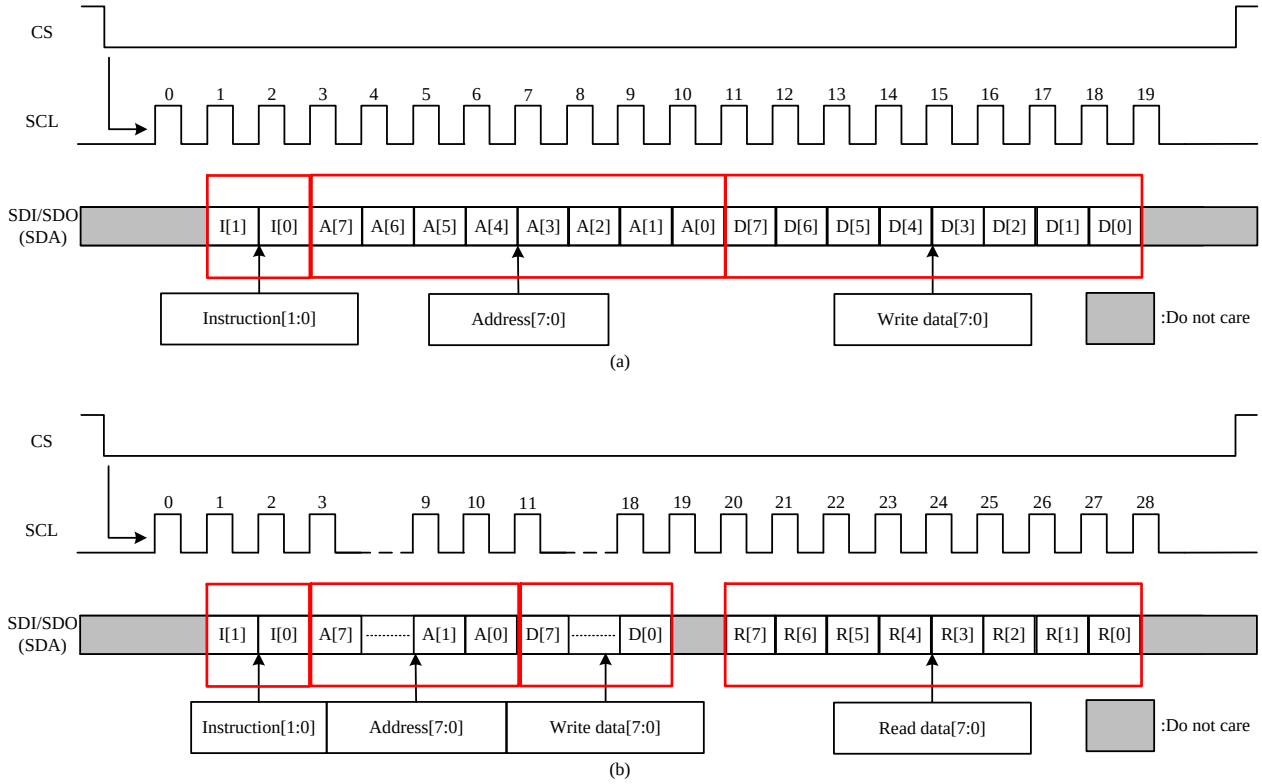


Fig. 2: Waveform of (a) 3-wire SPI protocol in procedure of writing data, (b) 3-wire SPI protocol in procedure of reading data.

Moreover, the proposed design also support the read out data from the slave device. Fig. 2 (b) shows the 3-wire SPI protocol in procedure of reading data. The procedure is added more serial clock to obtain the data from slave device. There are 29 serial clocks in this procedure. The read out code is 8bit (1byte) and transmitted in a serial type. Table I lists the SPI protocol command code for the proposed design. The 2 bits instruction code I[1] and I[0], individually, is controlled by the master device. Then, the length of SCL will be decided and fixed in proper number. Finally, the SPI protocol can be constructed successfully by the above mentioned.

Table 1: SPI protocol command code.

I [1]	I [0]	Mode	Length of SCL
0	0	Write	20
0	1	Read	29
1	-	-	-

Furthermore, the proposed SPI protocol is used in the field of VLSI application, it is necessary to have ability to communicate with huge number of slave device. Fig. 3 shows the one master device connected with multi-slave device. The master device can use CS port to specify the specific slave device to execute the 3-wire SPI protocol. By the proposed design, the slave device is suitable for mass production in VLSI technology.

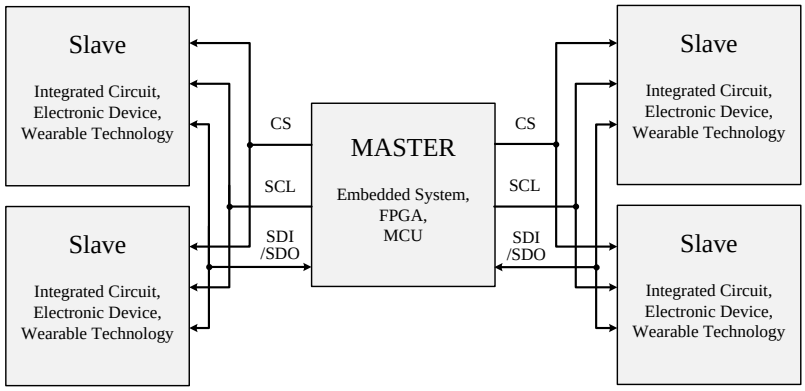


Fig. 3: One master device connected with multi-slave device.

3. Architecture of SPI Protocol

In order to develop the proposed SPI protocol in VLSI application, a master device and a slave device were created. The master device was implementation in FPGA. It consists of switches, buttons and general-purpose input/output (GPIO). The slave device was realize in ASIC design which is based on the VLSI technique. It includes a statistic random-access memory (SRAM) and a memory controller. The details of each module will be elaborated in the following:

3.1. Master Device (FPGA)

1. Switches and buttons

The switches, which are one of components in the FPGA, will be used as setting the instruction, address, and write data in the proposed design of master device. It totally needs 18 switches. It is composed of 2 bits instruction, 8bits address and 8bits writing data. Buttons are used to control the FPGA system. Moreover, one of button will trigger the CS port to start the SPI protocol after setting the switches with correct code. By using the switches and buttons components, the parallel data will be pre-set for the proposed FPGA design.

2. General-purpose input/output (GPIO)

After push the start button, the proposed FPGA device transmits signal in 3-wire SPI protocol to the slave device by general-purpose input/output (GPIO) components. The transmission procedure is converted parallel data, which is set by the switches on the FPGA, into serial type. Moreover, GPIO can also provide power supply to the slave device. Through the proposed design, the slave device can be communicate with FPGA device.

3.2. Slave Device (ASIC)

1. Statistic Random-Access Memory (SRAM)

A single-port statistic random-access memory (SRAM), which is provided by Artisan standard library, is used to store the data in the proposed ASIC design. Because the SRAM is a kind of volatile memory, the data will be erased by removing power supply which is connected on the proposed design. The data in SRAM will be changed, if the SPI protocol command instruct the write mode. Similarly, the data in the SRAM also can be read out, if the SPI protocol command instruct the read mode. The size of memory address and memory data are both 8 bit. By adding the memory in the proposed ASIC design, the memory data can be updated by the SPI interface.

2. Memory Controller

Since the proposed ASIC design includes a memory and needs to process the procedure of SPI protocol, a memory controller is added to access data in real time. The memory controller receives serial data and decode the instruction which was sent by the master device. Then, the controller controls in read/write action and loads/stores data from/into SRAM device. It provides an efficient way to process data between the SPI interface and internal memory.

4. Experimental Results

To verify the proposed architecture of 3-wire SPI protocol design, Fig. 4 shows the measurement environment including FPGA board, oscilloscope and the proposed ASIC design. An Altera DE2-115 development board with Cyclone IV core was used to emulate the proposed master device and the ASIC design was used a standard 0.18 μm CMOS technology and fabricated by the TSMC (Taiwan Semiconductor Manufacturing Co., LTD). An Agilent oscilloscope DSO7032A was

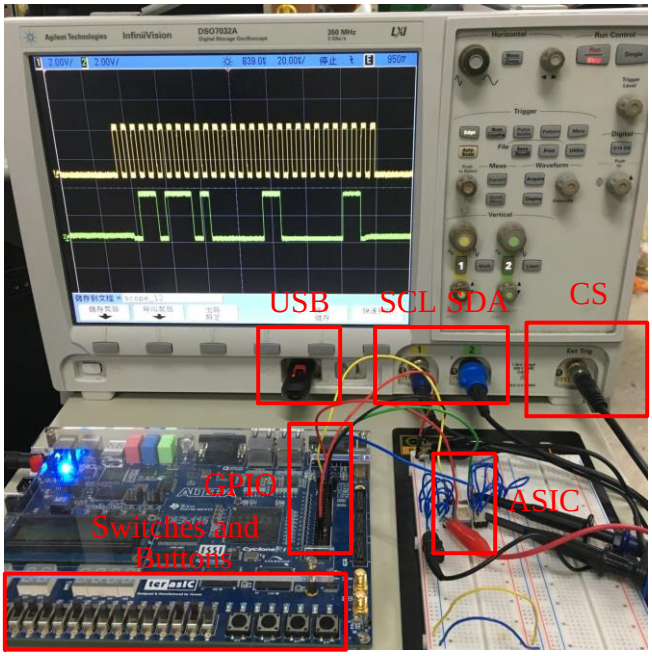
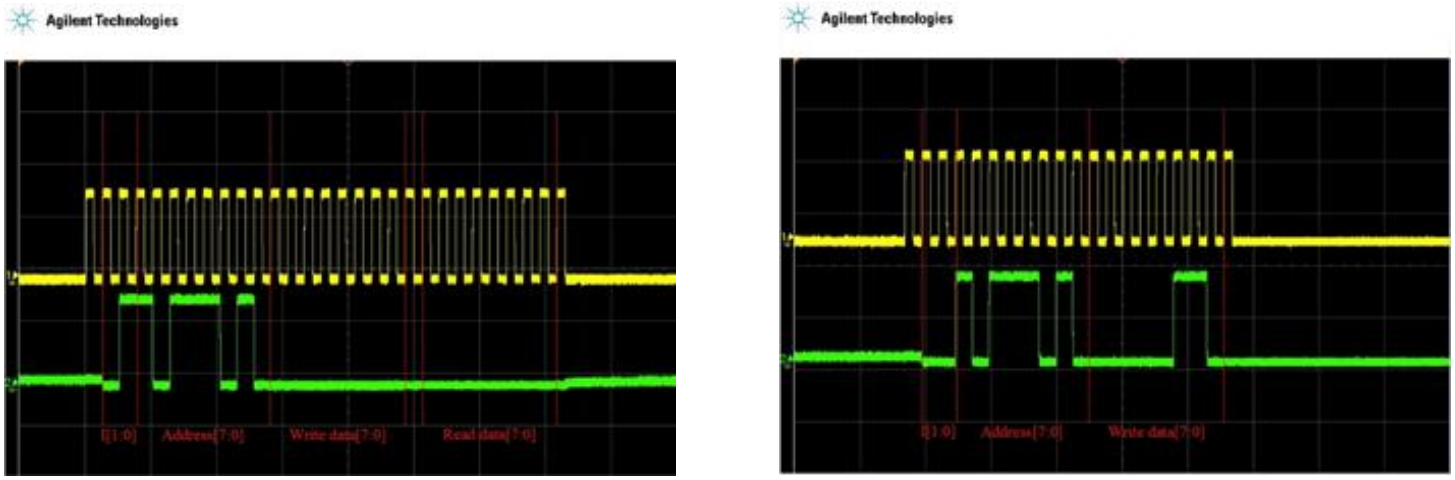


Fig. 4: Measurement environment including FPGA board, oscilloscope and ASIC design.

used to record the signals between the FPGA board and ASIC design. It measures the procedure of the SPI protocol. To be able to observe the measured signal and test the function of SPI protocol, the information of LCD

connected with oscilloscope can also be stored by the universal serial bus (USB) device. Firstly, the switches defined the read mode with SPI protocol command code, the data of memory address and write data by the designer. Fig.5 (a) shows the SPI protocol reading out initial data from slave device (26'b01_1011_1010_0000_0000_0000_0000). Then, the switches defined the write mode with SPI protocol command code, the data of memory address and write data by the designer. Fig.5 (b) shows the SPI protocol writing new data to slave device (18'b00_1011_1010_0000_0110). Finally, the switches defined the read mode again. Fig.6 shows the SPI protocol reading out written data from salve device (26'b01_1011_1010_0000_0110_0000_0110).



(a) (b)

Fig. 5: (a) SPI protocol reading out initial data from slave device, (b) SPI protocol writing new data to slave device.

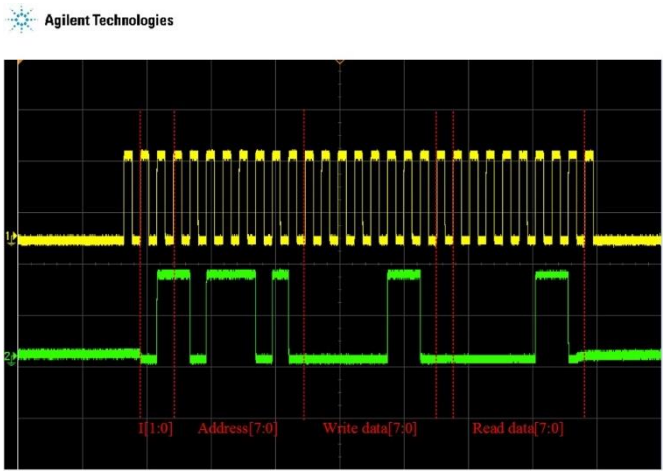


Fig. 6: SPI protocol reading out written data from salve device.

Table 2 lists the specification of proposed ASIC design. This work was used a TSMC 0.18 μm CMOS process technology. The voltage of Pad/Core are 3.3 and 1.8 V, respectively with maximum power consumption of 19 mW, system clock is 50MHz and the serial clock is 1MHz. The number of PAD are totally 18 and its chip size is 690 × 655 μm2. In addition, because the proposed ASIC design uses SRAM in the core of chip, the number of address is 256 and the data width is 8 bit. The cell area of SRAM is 44134 and the physical size is 215 × 206 μm2. Fig.7 shows the micrograph of the proposed ASIC using TSMC 0.18 μm CMOS. In summary, this work implemented the SPI protocol in VLSI technology and is suitable for various VLSI applications.

Table 2: Specification of proposed ASIC design.

Parameter	Specification	
Technology	TSMC 0.18 μm CMOS process	
Pad/Core Voltage	3.3/1.8 (V)	
Power consumption	19 mW	
System Clock	50 MHz	
Serial Clock	1 MHz	
Chip Size (μm^2)	690 × 655	
Number of Power/ Signal PAD	14/4	
	Memory	**Full Chip**
Cell area	44134	51376
Gate Counts (K)	4.4	5.1
Core Size (μm^2)	215 × 206	235 × 272

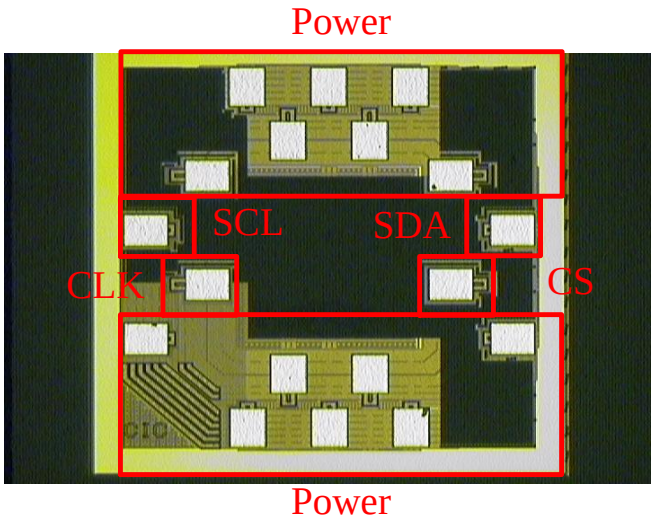


Fig. 7: Micrograph of the proposed ASIC using TSMC 0.18 μm CMOS.

5. Conclusion

A practical 3-wire SPI protocols for the VLSI applications and electronic device is presented in this paper. It successfully implements the protocol by the FPGA device and Application-specific integrated circuit. The proposed ASIC design can operate at 50 MHz. Its gate counts and core area are 5.1 K and 235 × 272μm2, respectively. This design has the benefits of fewer pad, cost intention and low complexity for VLSI applications.

Acknowledgements

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