Proceedings of the 4th World Congress on Electrical Engineering and Computer Systems and Sciences (EECSS'18)
Madrid, Spain – August 21 – 23, 2018
Paper No. EEE 121
DOI: 10.11159/eee18.121

A PVT Insensitive CMOS Negative Resistance Circuit for Q-factor Enhancement of FBAR

Dongmin Kim, Seongjin Bae, Donggu Im
Division of Electronics Engineering, Chonbuk National University
Jeonju-si, Jollabuk-do, Republic of Korea
aksd5736@naver.com; tjdwls8126@naver.com; dgim@jbnu.ac.kr

Extended Abstract

In the frequency division duplex (FDD) system, the receiver (Rx) sensitivity is greatly degraded due to desensitization and cross-modulation distortion caused by a large transmitter (Tx) leakage power [1]. A large power signal from the power amplifier is leak into the receiver due to the finite Tx-Rx isolation characteristic of the duplexer and as a result desensitizes the receiver, makes a cross-modulation distortion in the frequency band of the jammer signal. Especially, because the frequency of the jammer signal is very close to that of the desired signal, the cross-modulation distortion component severely degrades the signal-to-noise ratio (SNR). The degradation of SNR becomes more severe as it passes through the RF active circuitry such as low noise amplifier (LNA) and mixer. In order to alleviate the stringent linearity requirement of the front-end circuits, an additional film bulk acoustic resonator (FBAR) filter with very sharp out-of-band (OOB) rejection characteristic is adopted at the back of the LNA in order to remove Tx leakage signal. However, this increases cost and requires more printed circuit board (PCB) space. Unfortunately, considering there is no center frequency tenability of the FBAR filter, the evolution from 4G to 5G makes this problem worse.

The high Tx-Rx isolation characteristic of the FBAR duplexer is highly required to reduce Tx leakage signal level and remove an additional FBAR filter. For this, the filter order should be increased, but this approach increases the insertion loss of the filter. Therefore, it is desirable to improve Q-factor performance of the FBAR itself in order to achieve high Tx-Rx isolation without increasing the filter order. Considering the Q-factor of the FBAR is determined by the impedance ratio between pass-band frequency and stop-band frequency [2], to minimize the impedance level at stop-band frequency is much more effective for increasing the Q-factor of the resonator. From the perspective of the process development, because the impedance level at stop-band frequency is limited by the inherent parasitic resistance component like acoustic scattering loss [3], this requires much complicated processing steps and severely increases the development cost and period.

In this paper, a process, voltage, and temperature (PVT) insensitive single-ended CMOS negative resistance circuit is proposed to cancel the inherent parasitic resistance and enhance the Q-factor of the FBAR. It is very important to keep constant value of the negative resistance because the circuit is prone to oscillate when the absolute value of the negative resistance is greater than that of the parasitic resistance. By adopting the common source amplifier with diode-connected load and proportional to absolute temperature (PTAT) current source to the single-ended positive feedback-based negative resistance circuit, the negative resistance value of the proposed circuit becomes quite stable over PVT variations. In the simulation under the typical corner conditions (tt, 1.2 V, 27°C), the proposed circuit shows a negative resistance value of -5.1 Ω at 2.06 GHz frequency with a power consumption of 4.7 mW at a 1.2 V supply. The variations of the negative resistance value by temperature (-40°C ~ 100°C) and process corner (ss ~ ff) are less than 0.4 Ω and 0.2 Ω, respectively. In order to verify the effectiveness of the proposed circuit, the equivalent circuit model of FBAR and 5th-order ladder type filter were established for the simulation, and then OOB rejection characteristic with and without the proposed negative resistance circuit were compared. In conclusion, the proposed negative resistance circuit improves OOB rejection characteristic by 22 dB with the noise figure (NF) degradation of only 0.2 dB in passband.

Acknowledgements

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2018R1A2B6008816).

References

[1] Barend van Liempd, et al., "A +70-dBm IIP3 Electrical-Balance Duplexer for Highly Integrated Tunable Front-End," *IEEE Trans. Microw. Theory Techn*, vol. 64, no. 12, Dec. 2016.

[2] M. El Hassan, et al., "Tunability of Bulk Acoustic Wave Filters Using CMOS Transistor: Concept, Design and Implementation", *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2010, pp. 241-244.

[3] Hassan M. Edrees, et al., "Monolithically Integrated CMOS-SMR Oscillator in 65 nm CMOS Using Custom MPW Die-Level fabrication Process," *IEEE J. Microelectromechanical Systems*, vol. 26. Issue. 4, Aug. 2017.