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Power-Gated Accelerator Platform for Dark Silicon

Yung-Cheng Ma
Department of Computer Science and Information Engineering, Chang-Gung University
258 Wen-Hua First Road, Kwei-Shan District, Taoyuan, Taiwan
ycma@mail.cgu.edu.tw

Extended Abstract

In recent years, the progress of semiconductor manufacturing technology causes the rising of leakage power on a chip [1] and breaks Dennard scaling [2]. We are expecting the coming of dark silicon era: lots of current switches will be deployed for power gating and over half of the chip area has to be powered off [3]. Various researchers proposed the design of heterogeneous architectures featuring accelerators for energy efficiency [4][6]. Here we present our on-going project for developing application-specific accelerators that improve energy efficiency through power gating. The accelerator is based on a VLIW architecture with distributed register files for energy efficiency. Power gating are deployed on execution slots as well as the distributed register files. To exploit energy efficiency of the architecture, we propose the instruction scheduling algorithm to reduce cross-slot operand transfer and control the power gating over execution slots and register files. With the help of the compiler optimization, we develop programming tools to reduce the energy dissipation according to the user-given performance demand. Our evaluation shows that the joint architecture and compiler design is effective to improve energy efficiency through power gating. The future work is to develop programming tools that helps the development of a custom instruction set and utilizing the power-gating technology.

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