

Analysis and Implementation of a Novel Ultra-High Step-Up DC/DC Converter

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Abstract - A novel ultra-high step-up power converter (UHSUPC) is proposed for wind input voltage range application in a renewable energy power systems. The proposed converter exhibits a much higher voltage conversion ratio without using the extremely large duty cycle. The voltage conversion ratio also has an extra factor of $1/(1-D)$ compared with all the high step-up converters proposed in the literature. It means that the voltage gain will increase more than twice as the duty ratio D is operated more than 0.5. The operating principle and state-state analysis are presented herein. Finally, a prototype of input voltage 40 V, output voltage 400 V, and output power 200 W prototype of the proposed converter is implemented to verify the theoretical analysis on the basis of the experimental results.

Keywords: ultra-high step-up, dc/dc converter, wide range

1. Introduction

Due to the growing population and the exhaustion of fossil fuel, many renewable energy sources, such as photovoltaic (PV), fuel cells [1-2], wind energy, hydraulic energy, biomass energy, geothermal energy, fuel cells, etc., have been widely used in electric grid system. A renewable energy distributed generation system is shown in Fig.1. The PV and fuel cells always generate a dc voltage lower than 40 V [3] due to the safety and reliability considerations in the household applications, and thus a high-efficiency and high step-up dc-dc converter is applied to provide a high voltage dc bus of 380-400 V, which is required for a single-phase 220 Vac utility grid for the grid-connected dc/ac inverter.

Generally, an ideal conventional boost converter operating with an extreme large duty ratio can offer a high voltage gain. Unfortunately, the voltage gain of a conventional boost converter with the existing of the parasitic series resistor of an inductor [4] will decrease as the increasing of duty ratio. To overcome this drawback, many high step-up converter topologies are thus designed and presented in the literature [5-16]. As a result, an ultra-high step-up power converter (UHSUPC) is also proposed herein as shown in Fig.2 for wind input voltage range application in a renewable energy power system. The advantages and characteristics of the proposed UHSUPC are presented in the following:

- (1) The proposed UHSUPC has a very high voltage conversion ratio without operating at extremely large duty cycle.
- (2) The proposed UHSUPC can be used for wide input voltage range application because the duty cycle does not have any limitations. The voltage gains of the proposed converter can reach 10 and 20 with $D=0.36$ and $D=0.56$, respectively.
- (3) The power switches exhibit lower voltage stresses, which are all smaller than the high output voltage.

To ensure that the proposed converter exhibits the aforementioned features, the operating principle and steady-state analysis are given. A 200 W/400 V output, 40 V input prototype is also built to test the performances herein.

2. Operating Principle

The proposed UHSUPC presented in Fig. 2 contains two switches S_1 , S_2 , which are driven complementarily with two small dead bands T_d to avoid a short circuit across the DC voltage source and to achieve the zero-voltage switching (ZVS) at turn on operation for main switches. Some assumptions are made as follows before describing the operating principle of the proposed UHSUPC in a steady state.

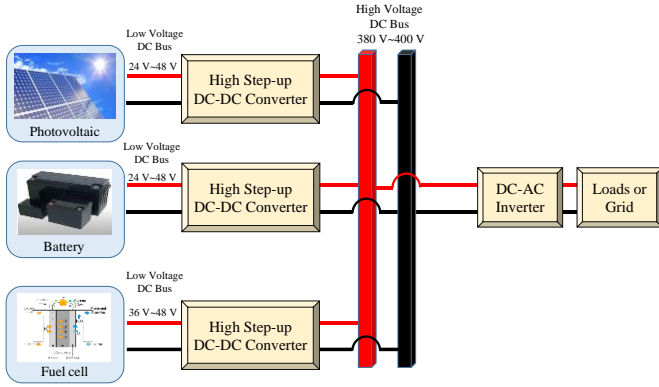


Fig. 1: Renewable energy distributed generation system.

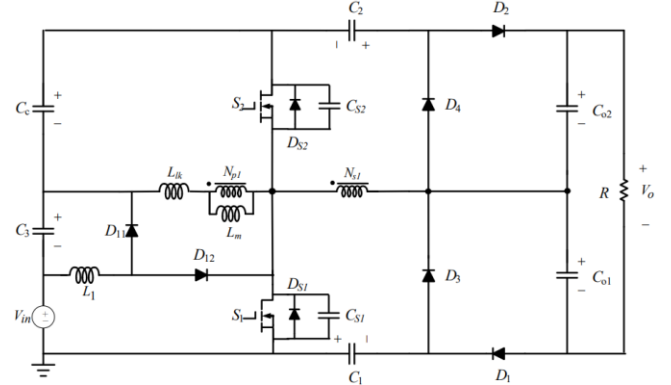


Fig. 2: Proposed UHSUPC.

- (1) The proposed converter is operated in continuous conduction mode (CCM).
- (2) All switches and diodes of the proposed UHSUPC are ideal. The switching time of the switches and the reverse-recovery time of the diodes can be neglected.
- (3) The boost capacitances (C_1, C_2, C_3, C_c) and output capacitances (C_{o1}, C_{o2}) are large enough so that their voltages are regarded as constant voltages $V_{c1}, V_{c2}, V_{c3}, V_{Cc}, V_{Co1}, V_{Co2}$ and V_o , respectively.
- (4) Because the time intervals of the resonances and charge/discharge times of capacitors C_{S1} and C_{S2} are much smaller than the switching period T_s , the inductor currents are considered as constants during the turn-off and turn-on transitions.
- (5) The turns ratio $n = N_{s1} / N_{p1}$ of the transformer is 1.

Based on the switching of the switches and diodes, the proposed converter operating over one switching period T_s can be divided into ten linear modes described as follows. The equivalent circuit of each stage is presented in Fig. 3.

Mode 1 [$t_0 \sim t_1$]: [S_1 :off, S_2 :off, D_1 :off, D_2 :on, D_3 :on, D_4 :off, D_{11} :off, D_{12} :on]

The equivalent circuit of this mode is depicted in Fig. 3(a). This mode is started as the switch S_1 is turned off at $t = t_0$, and the switch S_2 is still off. The leakage inductor current i_{Llk} continues to charge the capacitor C_{S1} and simultaneously to discharge the capacitor C_{S2} of the switch S_2 . When the voltage v_{ds1} increases from zero to $V_{in} + V_{c3}$, the diode D_{12} switches from on state to off state. The diode D_{11} also becomes forward-biased simultaneously. At this time, this mode ends.

Mode 2 [$t_1 \sim t_2$]: [S_1 :off, S_2 :off, D_1 :off, D_2 :on, D_3 :on, D_4 :off, D_{11} :on, D_{12} :off]

The voltage v_{ds2} still drops in this mode. As it falls to zero, the body diode D_{s2} of the switch S_2 is turned on. After that, the switch S_2 can be thus turned on under ZVS operation, and this mode finishes. The equivalent circuit of this mode is shown in Fig. 3(b).

Mode 3 [$t_2 \sim t_3$]: [S_1 :off, S_2 :on, D_1 :off, D_2 :on, D_3 :on, D_4 :off, D_{11} :on, D_{12} :off]

Fig. 3(c) depicts the equivalent circuit of the mode 3. At this mode, the leakage inductor current i_{Llk} starts to decrease because the negative voltage across the leakage inductor L_{lk} . When i_{Llk} drops and is equal to the magnetizing inductor current i_{Lm} , the diodes D_1 and D_4 become forward-biased, and the diodes D_2 and D_3 are switched from on to off. At this time, mode 3 also ends.

Mode 4 [$t_3 \sim t_4$]: [S_1 :off, S_2 :on, D_1 :on, D_2 :off, D_3 :off, D_4 :on, D_{11} :on, D_{12} :off]

The leakage inductor current i_{Llk} remains to decrease. As it drops to zero, this mode finishes. The equivalent circuit of this mode is demonstrated in Fig. 3(d).

Mode 5 [$t_4 \sim t_5$] : [S_1 :off \(\ S_2:on \(\ D_1 :on \(\ D_2 :off \(\ D_3 : off \(\ D_4 : on \(\ D_{11} : on \(\ D_{12} : off]

The leakage inductor current i_{Llk} becomes negative in this mode. When the switch S_2 is turned off, this mode ends. The equivalent circuit of this mode is shown in Fig. 3(e).

Mode 6 [$t_5 \sim t_6$] : [S_1 :off \(\ S_2 :off \(\ D_1 :on \(\ D_2 :off \(\ D_3 : off \(\ D_4 : on \(\ D_{11} : on \(\ D_{12} : off]

The equivalent circuit of this mode is depicted in Fig. 3(f). The leakage inductor current i_{Llk} is negative and started to discharge the capacitor C_{S1} and simultaneously to charge the parasitic capacitor C_{S2} . When the voltage v_{ds1} across the switch S_1 decreases to V_{in} , the diode D_{12} and D_{11} become forward-biased and reverse-biased, respectively. This mode is thus ended.

Mode 7 [$t_6 \sim t_7$] : [S_1 :off \(\ S_2 :off \(\ D_1 :on \(\ D_2 :off \(\ D_3 : off \(\ D_4 : on \(\ D_{11} : off \(\ D_{12} : on]

The voltage v_{ds1} still drops in this mode. However, the current i_{L1} will flow through the capacitor C_{S1} , the voltage v_{ds1} may be charged and cannot continue to drop. It means that the switch S_1 can just be turned on under quasi zero voltage switching (QZVS), and this mode finishes. The equivalent circuit of this mode is shown in Fig. 3(g).

Mode 8 [$t_7 \sim t_8$] : [S_1 :on \(\ S_2 :off \(\ D_1 :on \(\ D_2 :off \(\ D_3 : off \(\ D_4 : on \(\ D_{11} : off \(\ D_{12} : on]

Fig. 3(h) depicts the equivalent circuit of this mode. At this mode, the leakage inductor current i_{Llk} starts to increase because the positive voltage across to the leakage inductor L_{lk} . The leakage inductor current i_{Llk} remains to increase from negative value. As it increases to zero, the mode finishes.

Mode 9 [$t_8 \sim t_9$] : [S_1 :on \(\ S_2 :off \(\ D_1 :on \(\ D_2 :off \(\ D_3 : off \(\ D_4 : on \(\ D_{11} : off \(\ D_{12} : on]

The leakage inductor current i_{Llk} continues to increase from zero. When i_{Llk} increases and is equal to the magnetizing inductor current i_{Lm} , the diodes D_1 and D_4 become reverse-biased, and the diodes D_2 and D_3 are switched from off to on. This mode ends. The equivalent circuit of this mode is demonstrated in Fig. 3(i).

Mode 10 [$t_9 \sim t_{10}$] : [S_1 :on \(\ S_2 :off \(\ D_1 :off \(\ D_2 :on \(\ D_3 : on \(\ D_4 : off \(\ D_{11} : off \(\ D_{12} : on]

The leakage inductor current i_{Llk} still rises in this mode. When the switch S_1 is turned off, this mode ends and next ten modes for a switching period repeat again. The equivalent circuit of this mode is shown in Fig. 3(j).

As a result, the key waveforms over one switching period are schematically depicted in Fig. 4 based on the circuit analysis of the ten modes.

3. Converter Performance Analysis

A. Voltage Gain Expression

Based on the voltage-second balance principle of the inductor L_1 and magnetizing inductor L_m , it yields

$$V_{c3} = V_{in} \times \frac{D}{(1-D)} \quad (1)$$

and

$$V_{Cc} = V_{in} \times \frac{D}{(1-D)^2} \quad (2)$$

where D is the duty cycle of the power switch of S_1 . On the basis of the operating principle, the voltages across the output capacitors can be derived as follows. According to the equivalent circuits in mode 10 and mode 4 shown in Fig. 3(j) and Fig. 3(d), respectively, and Kirchoff's Voltage Law (KVL), one gets

$$V_{c1} = n(V_{c3} + V_{in}) \quad (3)$$

$$V_{Co2} = V_{c1} + V_{c2} + V_{c3} + V_{Cc} + V_{in} \quad (4)$$

and

$$V_{c2} = n \times V_{Cc} \quad (5)$$

$$V_{Co1} = V_{c1} + V_{c2} + V_{c3} + V_{Cc} + V_{in} \quad (6)$$

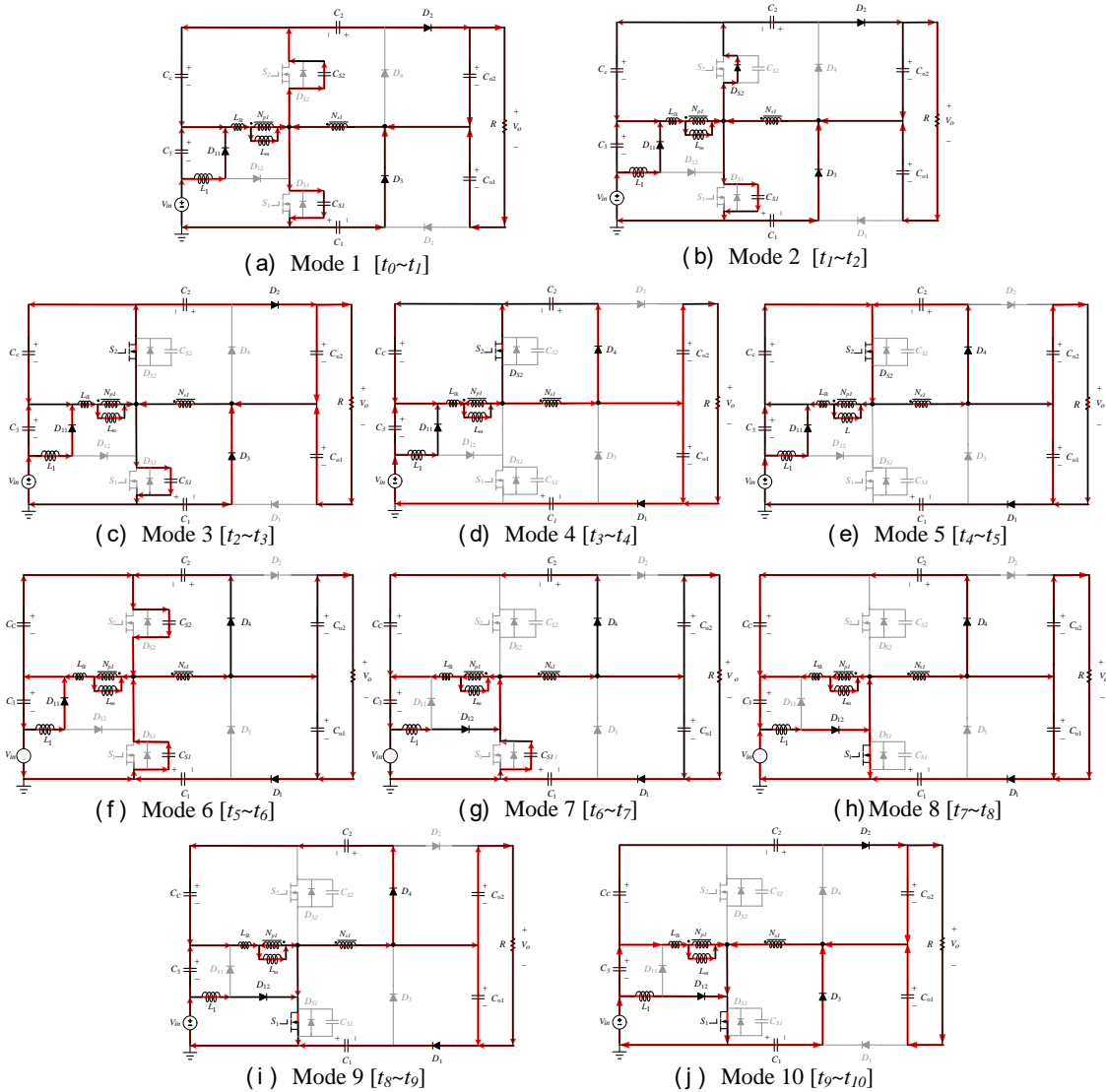


Fig. 3: Equivalent circuits for each mode of proposed UHSUPC.

Substituting Eqs. (1)-(3) and Eq. (5) into Eq. (4) and Eq. (6), thus we have

$$V_{Co1} = V_{Co2} = V_{in} \times \frac{(1+n)}{(1-D)^2} \quad (7)$$

Therefore, the output voltage of the proposed UHSUPC can be determined from Eq. (7) as

$$V_o = V_{Co1} + V_{Co2} = \frac{2(n+1)}{(1-D)^2} V_{in} \quad (8)$$

As a result, the voltage conversion ratio is derived as

$$\frac{V_o}{V_{in}} = \frac{2(n+1)}{(1-D)^2} \quad (9)$$

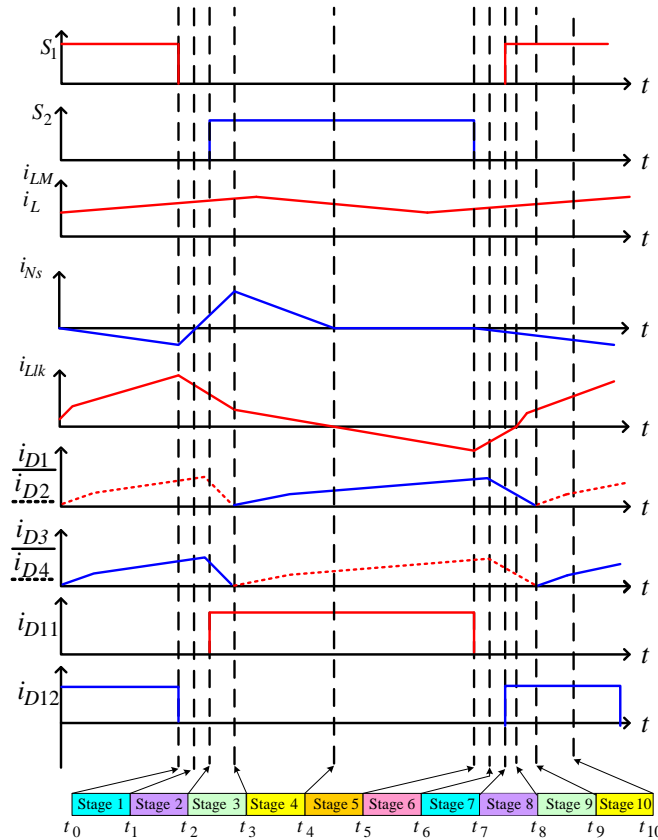


Fig. 4: Key waveforms of proposed UHSUPC.

According to Eq. (9), the voltage conversion ratio curves related to turns ratio n ($n=1, 2, 3$) and duty ratio D are derived and shown in Fig. 5. It reveals from Fig. 5 that the duty ratio 0.36 is applied to get the voltage conversion ratio 10 at a turns ratio $n=1$. It means that the proposed UHSUPC can achieve high step-up voltage conversion ratio without operating in an extreme duty cycle. Moreover, when the duty ratio is 0.56, it can also derive an ultra-high voltage gain of 20.

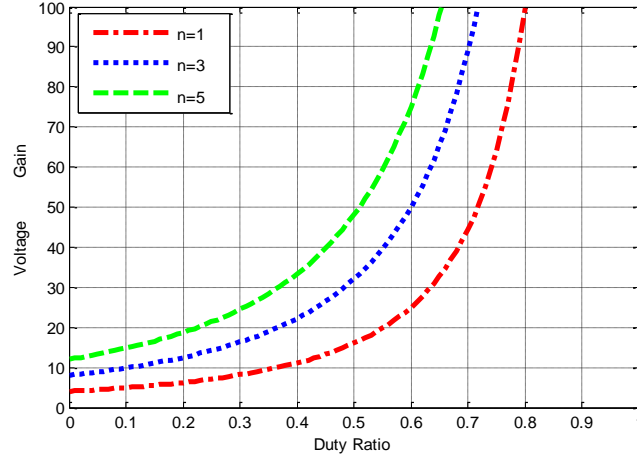


Fig. 5: Voltage conversion ratio curve versus duty cycle with various turns ratio.

B. Voltages across Power Switches and Capacitors

According to the operating principle, the voltage stresses across the power switches and diodes are given by

$$v_{DS(s_1)} = v_{DS(s_2)} = \frac{V_{in}}{(1-D)^2} = \frac{1}{2(1+n)} V_o \quad (10)$$

$$v_{D11(\max)} = v_{c3} = V_{in} \times \frac{D}{(1-D)} = \frac{D(1-D)}{2(1+n)} V_o \quad (11)$$

$$v_{D12(\max)} = v_{Cc} = V_{in} \times \frac{D}{(1-D)^2} = \frac{D}{2(1+n)} V_o \quad (12)$$

$$v_{D1(\max)} = v_{D2(\max)} = v_{D3(\max)} = v_{D4(\max)} = \frac{V_o}{2} \quad (13)$$

It reveals from Eqs. (10)-(13) that the voltage stresses across the power devices of the proposed UHSUPC are all lower than the output voltage. Therefore, it is compared with the conventional boost converter that the proposed UHSUPC has the less conduction losses and cost because the low-voltage-rated MOSFETs with low $R_{ds(on)}$ can be employed.

4. Experimental Results

A 200 W prototype of proposed UHSUPC with input voltage of 40V, output voltage of 400V and switching frequency of 100 kHz is built to validate the theoretical results. The power specifications and component parameters are listed in Table I. Fig. 6 shows that $V_{in}=40$ V and $V_o=400$ V are derived as the duty ratio D is about 0.4, which is approximated to the theoretical result of 0.36. It reveals that the high voltage gain is obtained without operating at an extremely large duty ratio. Fig. 7 depicts the waveforms of gating signals and the drain-source voltages of power switches. The voltage stresses of 102 V across the power switches are about one-fourth of the output voltage of 400 V.

Table 1: POWER SPECIFICATIONS AND COMPONENT PARAMETERS

V_{in}	40 V	V_o	400 V
P_o	200 W	f_s	100 kHz
n	1	L_m	200 μ H

C_1, C_2	10 μF	L_1	500 μH
C_c, C_{o1}, C_{o2}	47 μF	C_3	220 μF

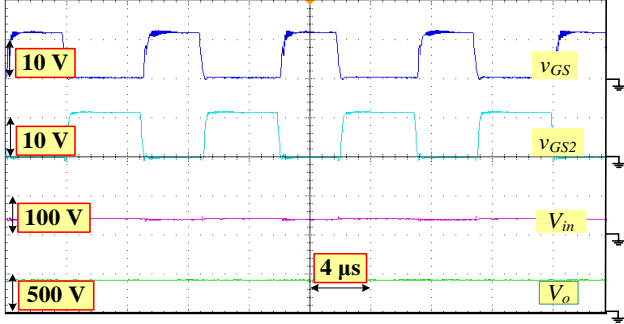


Fig. 6: Gating signals of switches and the input/output voltages.

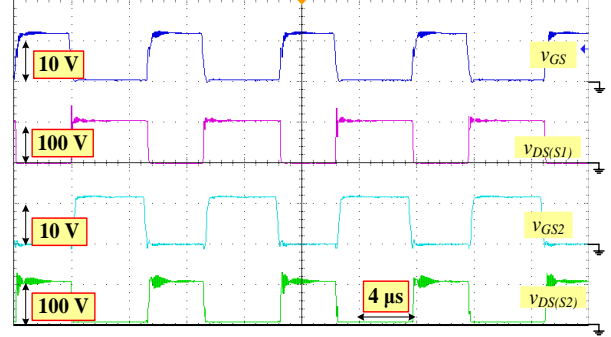


Fig. 7: Gating signals and the drain-source voltages of switches.

Fig. 8 shows that the experimental results of $V_{c3}=24.6\text{ V}$ and $V_{Cc}=45.2\text{ V}$, which are approximate to the theoretic results of $V_{c3}=26.67\text{ V}$ and $V_{Cc}=44.4\text{ V}$ from Eqs. (1)-(2) with $D=0.4$. Fig. 9 depicts that the experimental results of $V_{c1}=49.2\text{ V}$ and $V_{c2}=42.7\text{ V}$, which are also approximate to the theoretic results of $V_{c1}=44.6\text{ V}$ and $V_{c2}=44.4\text{ V}$ from Eq. (4) and Eq. (5), respectively, with $D=0.4$.

The voltage waveforms on the diodes (D_1, D_2, D_3 and D_4) and (D_{11} and D_{12}) are shown in Fig. 10 and Fig. 11. It reveals from Fig. 10 that all the voltages across diodes are close to $V_o/2$, which is 200 V. Based on Fig. 10, we get that the voltage stresses of diodes (D_{11} and D_{12}) are about $V_o/4$, which is 100 V.

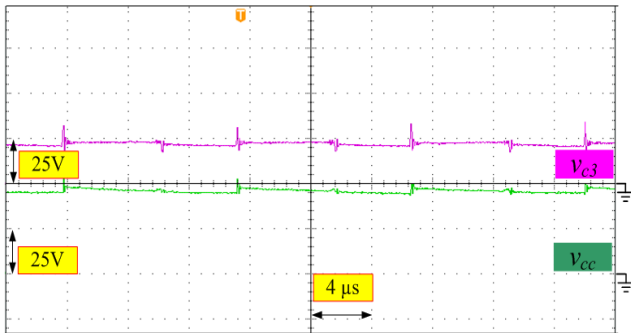


Fig. 8: Capacitor voltages of capacitors C_3 and C_c .

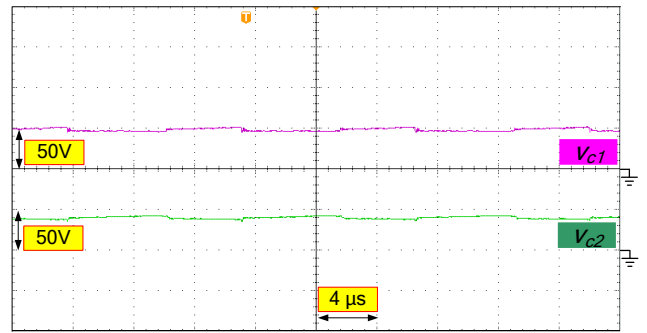


Fig. 9: Capacitor voltages of capacitors C_1 and C_2 .

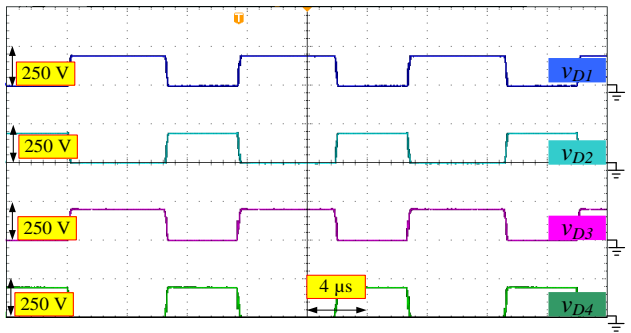


Fig. 10: Voltages of diodes D_1, D_2, D_3 and D_4 .

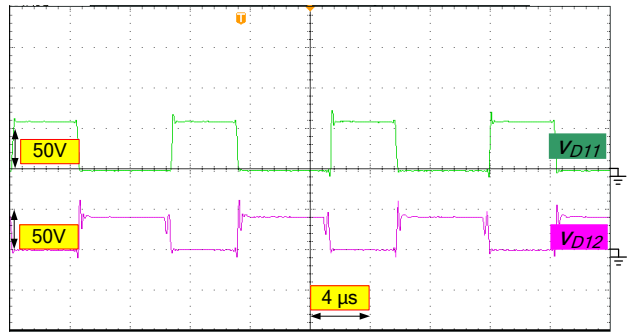


Fig. 11: Voltages of diodes D_{11} and D_{12} .

5. Conclusions

For a high step-up conversion application, a novel ultra-high step-up power converter (UHSUPC) is proposed in this paper. The operating duty ratio does not have the limitation, thus the proposed converter can be used for wide input voltage range applications. Based on the operating principle and steady-state analysis herein, it shows that the voltage gains of the proposed converter can reach 10 and 20 with $D=0.36$ and $D=0.56$, respectively. Moreover, the voltage stresses across all the power devices are much lower than output voltage. Finally, a 200 W prototype is implemented, and the theoretical results of the proposed UHSUPC are thus validated by experimental results.

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