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CMOS non-Foster Circuit Design Using 0.35µm BiCMOS Models by Cancelling the Parasitic Capacitances

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Abstract - In this paper, an improved type of CMOS non-Foster circuit with the cross-coupled pair is proposed to produce negative resistance, negative capacitance and negative inductance in the frequency range between 100 MHz and 3 GHz. Non-Foster circuits are also called negative impedance converter (NIC) circuits. The proposed NIC circuit is designed to eliminate the gate-source parasitic capacitances of NMOS transistors which are the core elements of this cross-coupled topology with the help of on-chip inductors. The negative impedance conversion capability of the NIC circuit is shown analytically with the detailed mathematical formulations and proofs. The circuit is also simulated and verified in AWR Design Environment using 0.35µm BiCMOS transistor models comparatively for two cases with and without LC tank sub-circuit. The circuit is tested and verified with the loads of 50Ω resistance, 5 pF capacitance and 10 nH inductance to be converted negatively. The improvement in the negative impedance conversion rate of the NIC circuit is presented clearly with the impedance-frequency curves. The results show that the performance of the proposed NIC circuit is satisfactory with the help of gate-source parasitic cancellation. Additionally, the preliminary on-chip IC component placement of the NIC circuit using 0.35µm BiCMOS models is proposed for the realization and production.

***Keywords*:** Non-foster, negative impedance, CMOS, RF, matching.

1. Introduction

Non-Foster circuits violate Foster's Reactance Theorem [1] as they produce circuit elements with negative impedance. This is because those kinds of circuits are attractive analog sub-circuit blocks with the capability of increasing the bandwidth and eliminating the parasitic effects in such kind of applications like electrically small antennas, power amplifiers, etc. The cross-coupled pair topology has been commonly used in negative impedance converter (NIC) circuits [2]. The CMOS implementation of the NIC circuit is first introduced by Brennan [3]. In Brennan's study, negative values of 100Ω, 220Ω, 470Ω and 1 kΩ resistive loads in HF band up to 10 MHz are obtained with around 20% deflections. CMOS based NIC circuit using current inversion technique is proposed in [4] for MOSFET-C integrator to increase its filtering performance with better phase response in HF band. A new method for realising the CMOS NIC circuit using unity gain cells which are composed of two current followers and one voltage follower is proposed in [5] to obtain -8 kΩ negative resistance which can be used in oscillator synthesis up to 1 GHz. The CMOS NIC principles introduced in [3] are applied in microwave frequencies up to 2 GHz using GaAS MMIC technology to produce negative resistance to compensate resonator losses of microwave resonator filters [6]. Negative capacitance realisation with 0,25 µm pHEMT process technology is first proposed by Kolev *et al* [7]. Negative inductance circuit which is separated from bias network using BiCMOS process is introduced in [8]. The circuit proposed in [8] is able to produce negative inductance which is tunable from -64 nH to -40 nH at UHF frequencies. Negative inductance CMOS circuit which is based on Linvill's work [11] is proposed in [9]. The cross-coupled CMOS technique is used in this study to generate -1 nH inductance in the frequency range between 0.1 and 6 GHz. On the other hand, the gate – source capacitance (C_{gs}) effects of cross-coupled NMOS transistors are not considered in the work referenced in [9]. The cross-coupled NIC circuits may also be used for impedance matching purposes in the design of RF power amplifiers. Thus, a broadband power amplifier based on GaN pHEMT ranging from 7 to 17 GHz using the matching capability of cross-coupled NIC circuit is realised in the work of Lee *et al* [10]. The negative capacitance ranging from -3pF

to -2pF is obtained for interstage matching by cancelling out the large input capacitance of the power amplifier. The C_{gs} effects is taken into consideration, but no solution is proposed to eliminate it in the design of NIC circuit referenced in [10]. There are also some other cross-coupled CMOS NIC circuits proposed in the literature [12] - [16]. However, none of those works proposes a solution for the destructive effects of C_{gs} in terms of the NIC circuits performance.

In this paper, a new design approach to obtain a cross-coupled CMOS NIC circuit eliminating the parasitic C_{gs} effects of NMOS transistors is presented. In the proposed circuit, double PMOS as active loads for each cross-coupled NMOS transistors are used. This helps in increasing the output resistance of the PMOS active loads which provide more realistic negative impedance conversion capability. The circuit also includes a current mirror sub-block to provide necessary bias currents to the cross-coupled NMOS transistors. Two inductors are added to the gates of each NMOS in series creating an *LC* resonant circuit together with C_{gs} so that X_C and X_L cancel each other out. It is the most important contribution of this study in realising the more efficient CMOS NIC circuits.

After the introduction and literature review, firstly theoretical analysis of the proposed NIC circuit is provided in Section II. And then the simulation and verification results performed in AWR Design Environment with 0.35μm BiCMOS transistor models together with the preliminary on-chip placement are given in Section III. Finally, the paper is summarized, and the future works are proposed accordingly in Section IV.

2. Theory and Analysis

The fundamental building block of the NIC circuits is cross-coupled pair of NMOS transistors which is shown in Fig. 1 below. It will be shown that the input impedance (Z_{AB}) of this circuit, which is the impedance between the terminals A and B, equals to the negative value of the load impedance, Z_L. So, it can written as

$$Z_{AB} = -kZ_L \tag{1}$$

where *k* is the negative impedance conversion rate of the NIC circuit. If $k \neq 1$, the value of the load may be adjusted as the expected negative impedance value at the input of the circuit. The coefficient k depends on many factors like circuit design approach, active/passive elements characteristics, etc.

The cross-coupled CMOS NIC circuit with *LC* tank which is proposed and designed in this work is shown in Fig. 2 below. The circuit can convert the load impedance (R8+R9, C8+C9 or L3+L4), which is placed between the drain terminals of M1 and M2 transistors, to its negative value and reflects this negative impedance on the input. NMOS transistors M1 and M2 are cross-coupled pair meaning that the gate terminal of M1 is connected to the drain of M2, and vice-versa. A transformer with centre tap is used at the input to provide two separate secondary voltages at the terminals 3 and 5 from a

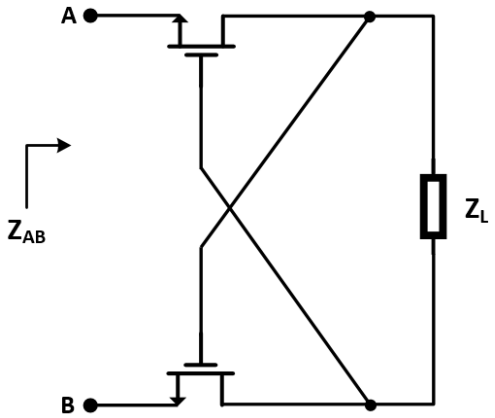

Fig. 1: The cross-coupled pair of MOSFETs as a core of the NIC circuits.

single-ended input at terminal 1. The ratios of secondary to primary turns of the transformer are given by n1 and n2. The circuit has a current mirror which is utilized by NMOS transistor M3. Drain currents of M1 and M2 are controlled through the current mirror. By adjusting the value of R7, the supply currents which are necessary for M1 and M2 can be set. In the current mirror sub-block, it can be written

$$\frac{I_{ref}}{I_{D1,D2}} = \frac{(W/L)_{M3}}{(W/L)_{M1}} = \frac{(W/L)_{M3}}{(W/L)_{M2}} \tag{2}$$

where I_{ref} is the current flowing in R7 and M3, the currents I_{D1} and I_{D2} are the currents flowing through M1 and M2 respectively. $(W/L)_{M1,M2,M3}$ are the aspect ratios of the NMOS transistors M1, M2 and M3 where W is the width of the channel, and L is the length of the channel. L1 and L2 are the inductors which are connected to the gate terminals of M1 and M2 to cancel the C_{gs} effects. C1-C4 are the DC block capacitors which separate the load impedance (R8+R9 or C8+C9 or L3+L4) from the DC conditions. R1 - R6 are DC biasing resistors which are connected to NMOS and PMOS transistors. R7 is the resistor to generate reference current flowing in the drain of M3 which utilizes current mirror sub-circuit.

For AC analysis, it can be redrawn the NIC circuit using the small-signal equivalent circuits of the NMOS transistors as shown in Fig. 3 below [17]. In this simplified model of the circuit, all DC sources, and related DC components i.e., the current mirror, PMOS active loads, and DC block capacitors are removed. The currents at the input and output stage can be written as $I_{i1} = I_{i2} = I_i$ and $I_{o1} = I_{o2} = I_o$ as it is a symmetrical circuit. If Kirchhoff Law is applied at the nodes S_1 and S_2,

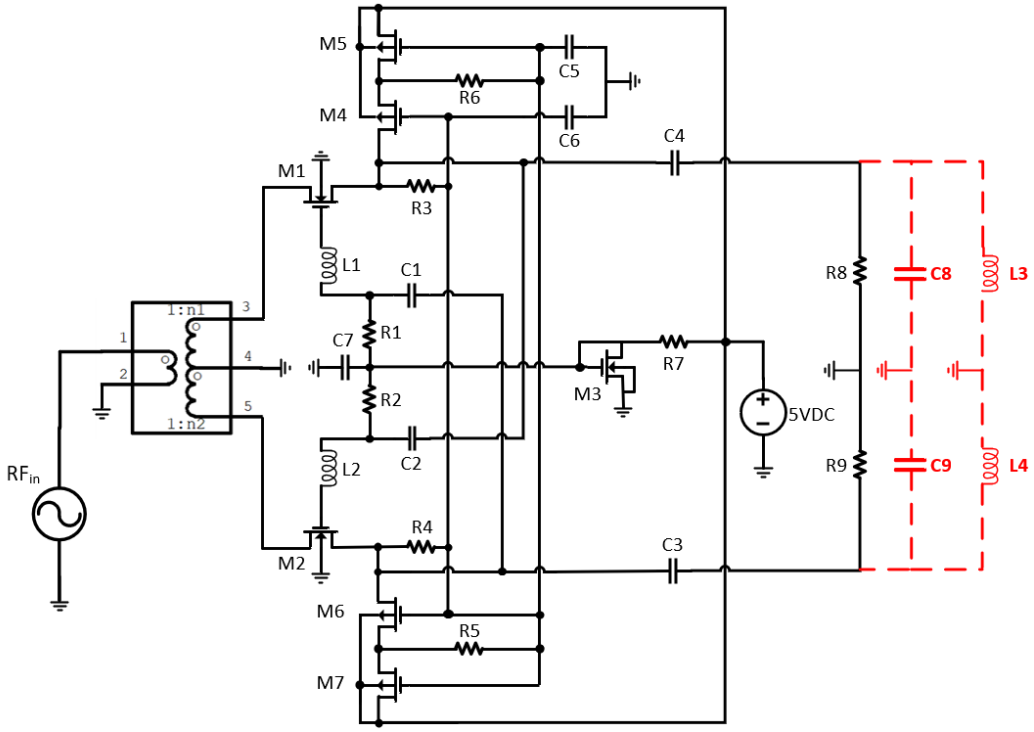

Fig. 2: The cross-coupled CMOS negative impedance converter circuit with serial LC tank.

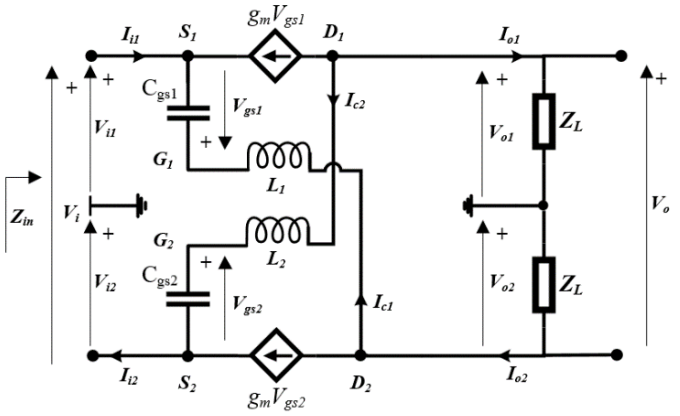

Fig. 3: Simplified model of CMOS NIC with the small-signal equivalent circuits of NMOS transistors.

the equations $I_{i1} + I_{cgs1} + g_m V_{gs1} = 0$, and $I_{i2} = I_{cgs2} + g_m V_{gs2}$ is obtained, where g_m is the transconductance of the NMOS transistors. It can easily be shown that

$$V_{gs1} = -\frac{V_{i1} + V_{o2}}{1 + s^2 L_1 C_{gs1}} \tag{3}$$

and

$$V_{gs2} = \frac{V_{i2} + V_{o1}}{1 + s^2 L_2 C_{gs2}} \tag{4}$$

where V_{gs1} and V_{gs2} gate-source voltages for M1 and M2 respectively, and s is the Laplace Operator. From (3) and (4), it can be modified the input currents I_{i1} and I_{i2} like in the following equations,

$$I_{i1} = (g_m + sC)\frac{V_{i1} + V_{o2}}{1 + s^2 L_1 C_{gs1}} \tag{5}$$

$$I_{i2} = (g_m + sC)\frac{V_{i2} + V_{o1}}{1 + s^2 L_2 C_{gs2}} \tag{6}$$

Summing those currents above in (5) and (6),

$$I_i = \frac{1}{2}\frac{(g_m + sC)}{1 + s^2 LC}(V_o + V_i) \tag{7}$$

assuming the inductors L_1, L_2 are equal, and the NMOS transistors are identical i.e., $C_{gs1} = C_{gs2}$. If the similar analysis for the output stage is repeated, it gives

$$V_o\left[\frac{1 + s^2 LC - (g_m - sC)Z_L}{1 + s^2 LC}\right] = \frac{g_m - sC}{1 + s^2 LC} Z_L V_i \tag{8}$$

Using (8) for V_o in (7) for I_i above, the following is obtained

$$I_i = \frac{1}{2}\frac{(g_m + sC)}{1 + s^2LC - (g_m - sC)Z_L}V_i \tag{9}$$

As a result, from (9) above, the input impedance, $Z_{in} = V_i/I_i$

$$Z_{in} = 2\frac{1 + s^2LC - (g_m - sC)Z_L}{g_m + sC} \tag{10}$$

In (10), it is known $s^2LC|_{S=j\omega_0} = -\omega^2LC|_{\omega=\omega_0=\frac{1}{\sqrt{LC}}} = -1$. So, Equation (10) for Z_{in} can be simplified as

$$Z_{in} = \frac{-2Z_L(g_m - sC)}{g_m + sC} = -2Z_L\frac{g_m\left(1 - j\frac{\omega C}{g_m}\right)}{g_m\left(1 + j\frac{\omega C}{g_m}\right)} \tag{11}$$

The cut-off frequency of NMOS, $\omega_F = g_m/C$, and $\omega/\omega_F = f/f_T \ll 1$, where f is the signal frequency applied in the circuit, f_T is the cut-off frequency. So, the equation for the input impedance of the circuit, Z_{in}, can be approximated as

$$Z_{in} \approx -2Z_L \tag{12}$$

where $-2Z_L$ is the total load which is equal to the series value of R8+R9 or C8+C9 or L3+L4 in the circuit shown in Fig. 2 above. In this theoretical circuit analysis, the coefficient k is equal to 1 as explained and shown in (1) above. This is the important result proving negative impedance conversion capability for the NIC circuit with the cancellation of the destructive effects of cross-coupled NMOS transistors' gate-source capacitance, C_{gs1} and C_{gs2}.

3. Verification of the Circuit

To verify the proposed NIC circuit's performance, it is simulated and characterized using 0.35μm BiCMOS models in AWR Design Environment. Pointer – Robust Optimization method is used to automatically adjust the designated circuit parameters such as MOSFET's width and length, passive circuit-element values, etc. Important design parameter values which are obtained from the optimization are given in Table 1 below for the simulated NIC circuit. The width of the gates of M1 and M2 are around 400μm. To reduce their gate widths, they are split into smaller ones. So, the number of gate fingers are selected as 40 for M1 and M2. The width of the gates of the PMOS transistors M4, M5, M6 and M7 are around 800μm. So, the number of gate fingers are selected as 80 for M4, M5, M6 and M7. In this way, the widths of the gates are reduced to 10μm for all those transistors. Only one gate finger is used for M3 as it has 9μm of the gate width.

The optimized parameter values given in Table 1 are realistic for on-chip implementation as they have moderate dimensions. In addition to the parameters shown in the table below, octagonal spiral inductor model for the inductors L1 and L2, metal-insulator-metal (MIM) capacitor model for C1 to C7, and n-well resistor model for R1 to R9 in the circuit with BiCMOS are used for the simulation. The input geometric parameters are selected for the octagonal spiral inductor to get 9.5 nH inductance approximately. So, the number of turns is 6, turn spacing is 2μm, turn width is 1μm, and the outer diameter is 150μm. The on-chip dimensions of resistors and capacitors are also given in Table 1 below. A step-down transformer with 1:0.5/0.5 turn ratios is also used in the AWR simulations, and it can be implemented on-chip easily [18].

Input impedance vs frequency curves for the proposed NIC circuit with BiCMOS transistor models including resistive, capacitive, and inductive loads are given in Fig. 4 below comparatively. Fig. 4a shows the negative resistance capability of

Table 1: Design parameters of the proposed NIC circuit with BiCMOS transistor models for AWR verifications.

Parameter	Value	Unit
Channel width (W) for M1, M2	400	µm
Channel length (L) for M1, M2	0.35	µm
Channel width (W) for M3	9	µm
Channel length (L) for M3	0.35	µm
Channel width (W) for M4, M5, M6, M7	800	µm
Channel length (L) for M4, M5, M6, M7	0.35	µm
Serial gate inductors (L1, L2)	9.5	nH
Turn ratios (n1, n2) of input transformer	0.5	-
DC block capacitors (C1, C2, C5, C6, C7)	3	pF
Width of C1, C2, C5, C6, C7	50	µm
Length of C1, C2, C5, C6, C7	40	µm
DC block capacitors (C3, C4)	20	pF
Width of C3, C4,	115	µm
Length of C3, C4	115	µm
Current mirror resistor (R7)	4	kΩ
Biasing resistors (R1 to R6)	10	kΩ
Width of R1 to R6	5	µm
Length of R1 to R6	50	µm
DC power supply	5	VDC
Load resistors (R8, R9)	25	Ω
Load capacitors (C8, C9)	10	pF
Load inductors (L3, L4)	5	nH

the circuit for 50Ω resistive load with and without L1-L2 inductors. It can be clearly seen that if those inductors are used in the circuit, its negative inductance conversion ratio is improved as the input impedance is around -28Ω and -9Ω in 2.4GHz with and without the inductors respectively. The NIC circuit with parasitic cancellation inductors has better performance. The similar improvement is obtained for the capacitive load as shown in Fig. 4b below. The circuit converts 5pF capacitive load better to its negative value if the L1-L2 inductors are included in the circuit. The reactance of 5pF capacitive load in 2.4 GHz equals to -13.2Ω. The input impedance is measured +15.1Ω, and +8.2Ω in 2.4 GHz with and without inductors respectively. So, closer results are achieved with the inductors included. The similar improvement is seen in Fig. 4c for 10nH inductive load with the LC tank sub-circuit cancelling the parasitic effects.

4. Conclusion

In this work, a CMOS NIC circuit up to 3 GHz is designed with the elimination of gate-source parasitic capacitances of the cross-coupled NMOS pairs. It is analytically shown the negative impedance conversion capability of the circuit. The circuit is also verified in AWR Design Environment with BiCMOS models using resistive, capacitive, and inductive loads. The verification results showed that the designed NIC circuit converts the loads to their negative values at the input. The performance of the NIC circuit for resistive and capacitive loads are better than that of inductive load. The most important result and achievement is that the proposed NIC circuit provides better performance with the resonance inductors in terms of negative impedance conversion capability by cancelling the gate-source parasitic capacitances of NMOS transistors.

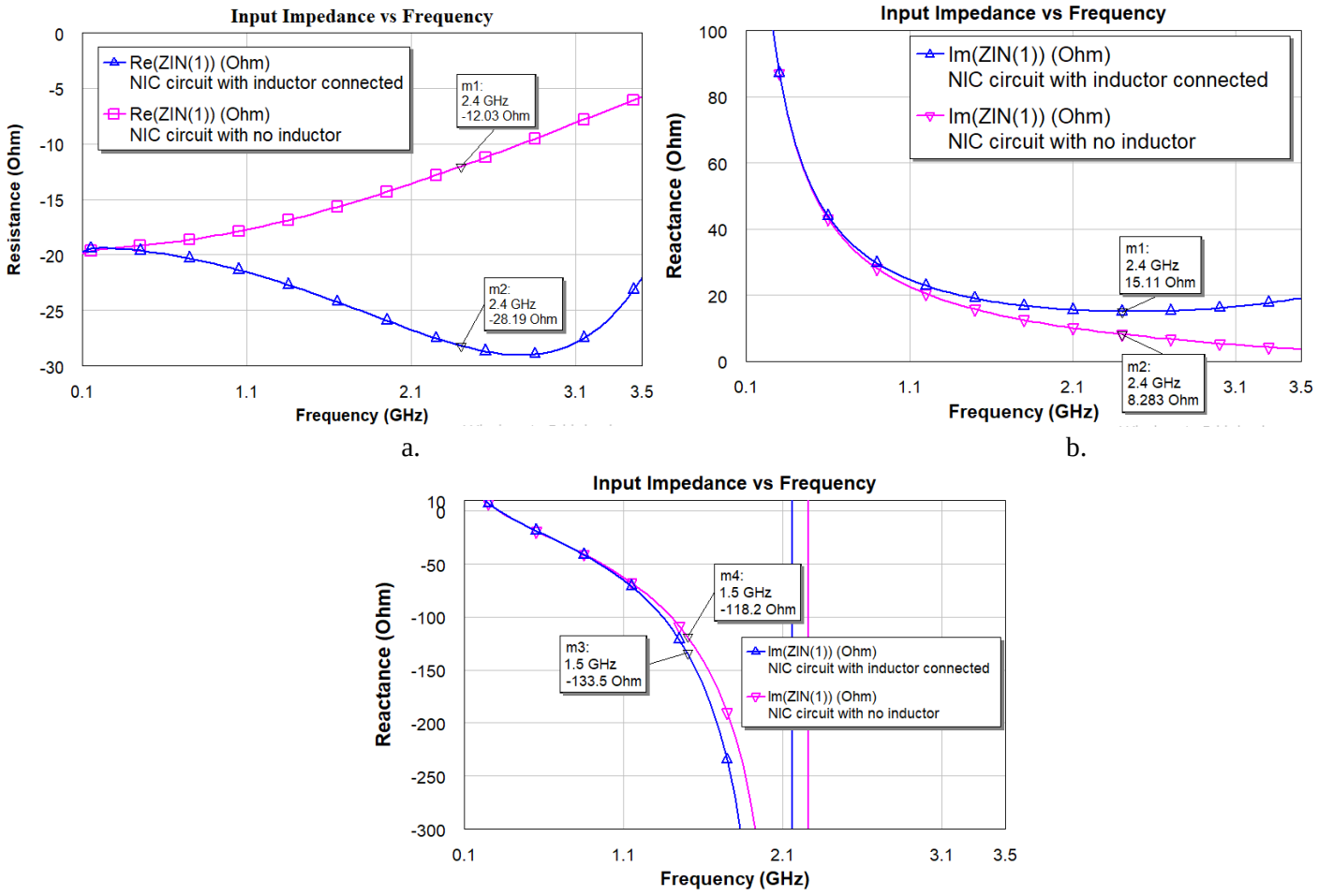

Fig. 4: Input impedance vs frequency curves for the NIC circuit with BiCMOS models. Blue curves show the input impedances of the NIC circuits with L1-L2 inductors connected while pink curves show the input impedances of the NIC circuits with L1-L2 inductors unconnected. a. NIC circuit with 50Ω load. b. NIC circuit with 5pF load. c. NIC circuit with 10nH load.

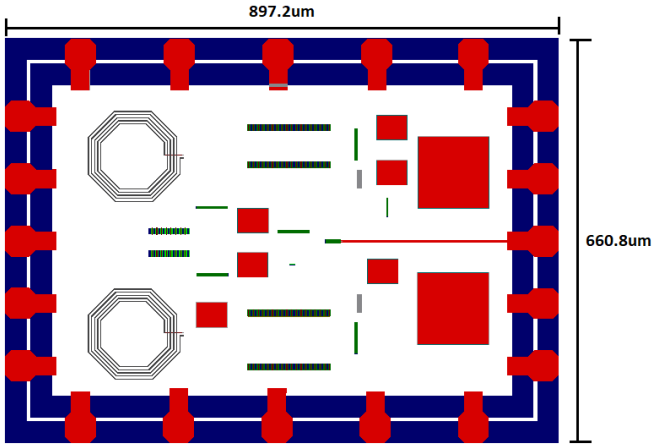

Fig. 5: Preliminary on-chip placement of the proposed NIC circuit.

Physical layout work with 0.25μm CMOS process for this NIC circuit is still ongoing, and its production is scheduled. The preliminary on-chip placement of the proposed NIC circuit is also shown in Fig. 5 above. Test results of the produced CMOS NIC IC will be presented in the next paper with the comparison of simulated results. The proposed NIC circuit can be used as an interstage matching block in the design of RF power amplifiers (PA) to increase their bandwidth [10]. With the help of NIC circuits, the effect of the high input capacitance which restricts the bandwidth in PA's, can be highly reduced. This kind of NIC circuits generating negative resistance can also be used in the oscillator circuits to increase their tuning range [19]. Henceforth, any kind of circuits requiring broadband matching can be designed with this type of NIC circuit.

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