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Critical Paths Selection for Delay Faults

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Extended Abstract

Right timing of complex digital circuits and systems in nanotechnology need careful design steps and testing. Incorrect timing can be caused during design or manufacturing processes. Incorrect timing is manifested as delay faults. The delay faults in digital circuit testing are more and more important due to huge number of gates and lines integrated on a chip specifically in nanotechnologies. Some test vectors have to be prepared for delay faults testing depending on fault models. Various fault models exist for test vectors generation from which the gate delay fault model, the transition fault model and the path delay fault model are basic models for time specification testing. The paths delay faults are crucial for nanotechnologies based on their tiny geometries in digital integrated circuits. These faults are tested only via selected critical paths in a tested digital circuit because huge number of paths exists in its structure. Nowadays, the critical paths are specified e.g. by static timing analysis (STA), dynamic timing analysis (DTA) and others. During last decade new aspects have been recognized in critical paths selection. Many factors such as multiple input switching, power supply noise, type of propagated signal edge (rising, falling) and others affecting the signal delay propagation and thus they can increase path criticality (Wu et al., 2010). The impact of each parameter to the path delay faults has been solved and published in some papers by (Dobai et al., 2010), (Wu et al., 2008) and (Metzler et al., 2013) but their joint effects should be also investigated. The paper presents a new method and a new formula for evaluation of paths criticality. The method contributes to higher delay fault coverage in digital circuits. Experiments over benchmark circuits have proved effectiveness of the method and its implementation to an automatic system for critical paths selection based on multiple parameters effects.

A new general method for critical path selection has been developed and implemented based on influence on multiple parameters, STA, DFT and new defined formula. The main idea is sort a list of critical paths founded by STA using the new defined requirement – path criticality for increasing path delay fault coverage. Path criticality c_p based on multiple parameters is expressed by formula:

$$c_p = \left(1 - \frac{s_p}{t}\right) \cdot \prod_{j=1}^{k} \left[1 - w_j \left(1 - i_{jp}\right)\right] \tag{1}$$

where s_p is the slack for path p from STA, k represents the number of accepted parameters on which criticality depends, t represents length of time interval, w_j is weight of parameter j and i_{jp} represents calculated index of parameter j impact on path p. Each critical path received from STA is evaluated by the path criticality and according it is a new set of critical paths established for testing path delay faults.

Maximal impact of all parameters together is 20 % which is based on previous published results. Parameters with impact to delay fault criticality are multiple input switching, test robustness, asymmetric transition delay, number of don't care values in test vectors, paths used in the functional mode, power supply noise (Rao at al., 2013), through silicon vias, power consumption, aging factor and others. Some critical paths can be found as untestable based on structure of the circuit. In addition the circuit structure can be modified to increase the number of testable critical paths by some design-for-testability (DFT) techniques

(Pomeranz and Reddy, 2008). A more effective DFT technique for changing untestable critical paths to testable has been developed and integrated in the proposed automatic system for critical paths selection named PaCGen (**Pa**rameterized **C**ritical paths **Gen**erator).

Experiments using the PaCGen system were done over sequential digital benchmark circuits (ISCAS-89 benchmarks) and they proved effectiveness in delay fault coverage. The received results together with basic blocks of PaCGEN will be shown during presentation at the conference. The STA data for used digital benchmark circuits in experiments was received by synthesis using Cadence Encounter RTL Compiler with 45 nanometre technology with NanGate FreePDK45 Generic Open Cell Library. The proposed and implemented method for critical path selection based on multiple parameters shows up to 2.63 % better path delay fault coverage on the circuits. In combination with DFT method (Siebert and Gramatova, 2013), transition faults coverage was increased up to 16 %. Quality improvement on the path delay fault model was more than 5 %. The methods and complete results are involved in the Dissertation Thesis. The new method and the system PaCGen contribute to the delay faults testing, important mainly for nanotechnologies. Future works is oriented to find specific weights for used multiple parameters and their influence to criticality of paths in manometers digital circuits.

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Dobai, R., & Balaz, M. (2013). SAT-Based Generation of Compressed Skewed-Load Tests for Transition Delay Faults. *Microprocessors and Microsystems*, *37*, 196-205.

Metzler, C., Todri-Sanial, A., Bosio, A., & Dilillo, L. (2013). Computing Detection Probability of Delay Defects In Signal Line Tsvs. *Proc. of European Test Symposium ETS*, 1-6.

Pomeranz, I., & Reddy, S. M. (2008). Design-For-Testability for Improved Path Delay Fault Coverage of Critical Paths. *Proc. of 21st International Conference on VLSI Design*, 175-180.

Rao, S.K., Robucci, R., & Patel, C. (2013). Scalable Dynamic Technique for Accurately Predicting Power-Supply Noise and Path Delay. *Proc. of VLSI Test Symposium*, 1-6.

Siebert, M., & Gramatova, E. (2013). Delay Fault Coverage Increasing In Digital Circuits. *Proc. of Euromicro Conference on Digital System Design*, 475-478.

Wu, S.H., Chakravarty, S., Tetelbaum, A., & Wang L. C. (2008). Refining Delay Test Methodology Using Konwledge of Asymmetric Transition Delay. *Proc. of Asian Test Symposium*, 137-142.

Wu, S.H., Chakravarty, S., & Wang, L. (2010). Impact of Multiple Input Switching On Delay Test under Process Variation. *Proc. of VLSI Test Symposium*, 87-92.