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PSPICE Analysis of CNFET Based Logic Circuits for Low Voltage Applications

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Extended Abstract

There are many technological limitations have been occurring with existing MOSFET technologies. In order to maximize the performances of silicon-based circuits, we have to achieved its physical limitations. Special characteristics of carbon nanotube (CNT) such as high on/off current ratio, high mobility of electrons, and their unique one dimensional band structure that suppresses back scattering and ballistic operation have made it as a potential replacement for silicon MOSFETs [1-3]. Because of the I-V characteristics of CNTFETs are closely similar to silicon MOSFET, most of MOS-based circuits can be transformed to a CNTFET based design. In comparison with MOSFET carbon nanotubes field effect transistors (CNTFETs) have less space and more scalability and this feature made them suitable for displacing of this technology. These transistors use carbon nanotubes as their channel. Less power and high velocity of this transistor, have encouraged the digital circuit designers to use these transistors for their designs [2,4]. Recently, the designers handle CNTEFTs in their designs, such as multiple valued reasonable circuits, accounted circuits, investors and other logic circuits. In past decades the binary logic is used in computational circuits. In recent decades MVL is considered as an alternative to the common binary logics. The use of CNTFET technology to directly transpose existing CMOS-based logic structures proved experimentally both with resistive-load gates and complementary logic. Specific CNTFET properties have also been used in multiple-valued logic.

In this research, advantages of CNFET technology over the existing CMOS technology is presented. The SPICE circuit simulator has been used to simulate CNFET based logic circuits. The logic circuits of CNFETs and Hybrid are simulated using 32nm CNFET technology. For simulation CNFET-based logic circuits, the compact model is used. Circuits are compared by power consumption, propagation delay and power delay product (PDP). The proposed design is compared with MOSFET designs. The CNFETs are simulated in condition of 0.30v power supply.

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