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2.4GHZ Class F Power Amplifier for Wireless Medical Sensor Network

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Abstract - The objective of this research was to design a 2.4 GHz class F Power Amplifier (PA), with 0.18um Semiconductor Manufacturing International Corporation (SMIC) CMOS technology by using Cadence software, for sensor network, especially for health care. The ultimate goal for such application is to minimize the trade-offs between performance and cost, and between performance and low power consumption design. This power amplifier can transmit 18dBm output power to a 50Ω load. The power added efficiency is 46% at 1dB compression point and the power gain is 18dB, the total power consumption is 2.8W. The performance of the power amplifier meets the specification requirements of the desired.

***Keywords*:** two stage, class F, cascade, power amplifier

1. Introduction

An emerging application in nanotechnology is the field of nano-electronics. The field of nano-electronics leverages new methods and materials to build electronic devices with feature sizes on the nanoscale [1]. Complementary metal–oxide–semiconductor (CMOS) is mature technology that has a long history in integrated circuit fabrication. CMOS technology has been used to implement a vast array of devices critical to modern society. Some of the most ubiquitous applications include devices such as microprocessors, microcontrollers, static RAM, image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication applications.

The drive to miniaturize such devices has refined CMOS into a capable technology for fabricating nanotechnology devices. In the current technology, features less that 10nm across can be made. With these techniques and materials, billions of transistors can be fabricated on a wafer - allowing a vast array of functons to be integrated on a single chip. These qualities make CMOS is a strong process for fabricating nanoscale devices. There are some physical limitations to silicon-based processes, however, and there is room for improvement in the CMOS process for nano-fabrication applications.

Wireless sensor networks (WSN) are collections of distributed sensors which provide data about their environment. This data can relate to many applications, such as human body monitoring or environmental conditions - such as temperature, soil moisture, wind speed, or sound levels. Nodes in this network, after collecting data can then pass the collected data through the network to a central location. Contemporary networks are often bidirectional which enables the control of sensor activity, as well. Such networks are widely used in industrial and consumer applications, providing process monitoring and control, healthcare monitoring, and so on.

The basic architecture of a WSN is shown in figure 1. A WSN is composed of a few to several hundreds or even thousands nodes, where each node is connected to one or more sensors. A sensor network node typically has several parts: a radio transceiver with an internal or an external antenna, a microcontroller, and a battery or energy harvesting mechanism to provide energy.

Wireless medical sensor networks have offered significant improvements to the healthcare industry in the 21st century. Devices are arranged on a patient’s body and can be used to closely monitor the physiological condition of patients. These medical sensors monitor the patient’s vital body parameters, such as temperature, heart rate, blood pressure, oxygen saturation, and transmit the data to a doctor in real time [1]. When a doctor reviews the transmitted sensor readings, they can get a better understanding of a patient's health conditions. People living in rural areas would especially benefit, since 9% of physicians work in rural areas while almost 20% of the US population lives there [2]. A shortage of physicians and specialist is a big issue in such areas, even today. But Wireless Medical Sensor Network technology has the potential to alleviate the problem.

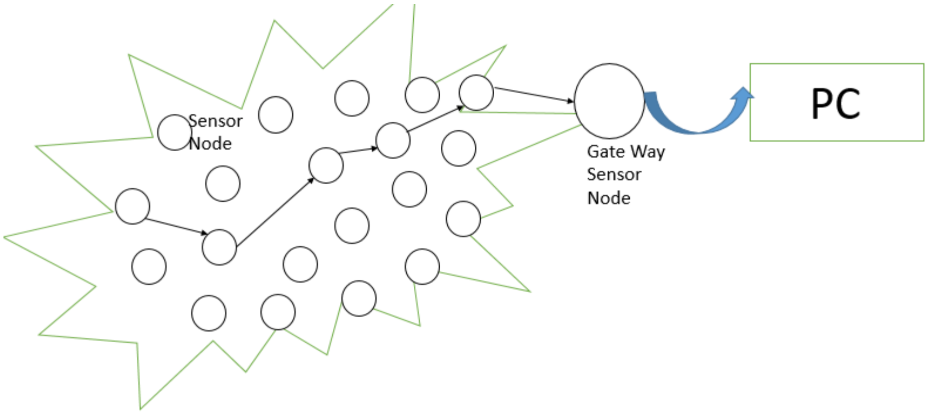

Fig. 1: Basic structure of a typical sensor node.

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2. Background Introduction

Fig.2 shows that the basic sensing node can collect the physiological signals (e.g.: such as EEG, ECG, body temperature, blood pressure, heart beat etc.), when attached to a human body [2]. The processing unit processes all the sensed signals, then sends out the data based on communication protocols [3] [4] [5] [6]. All the processed data will be transmitted through a wireless link to a portable, personal base-station. Doctors can then obtain all the patients’ data through the network. Two major requirements for a WSN are the need for a compact form factor and low cost. As seen in the figure 3, the power amplifier is the major consumer of power in a sensor node. A power amplifier design for a WSN would ideally be low cost while providing high gain, high linearity and low power consumption. This is a challenging design requirement. For instance, while silicon designs are low cost, amplifiers built in silicon do not typically provide high gain or linearity. Other LNA, Mixer and VCO talked at [7].

The rapid growth of wireless systems has created increasing demand of lower cost, smaller form factor systems with superior and complex functionalities. While III/V semiconductors, such as GaAs and SiGe, can easily achieve high power output and high gain, they incur high costs. Often to reduce cost, circuits designed are targeted for the CMOS process, since CMOS is a common and well-established process. For medical devices, the power amplifier is the main power consumer. For RF power amplifiers design, there is always a trade of PAE, power output and the supply voltage for different standards and applications. And for this proposal, a class F power amplifier is the main design under investigation. In order to meet the standards, the PA is designed as shown in table 1.

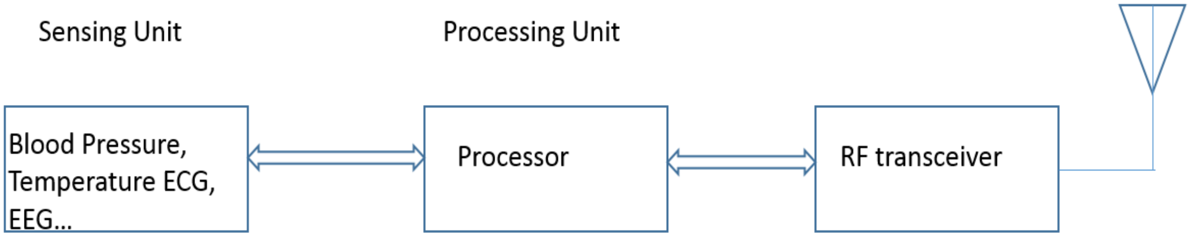


Fig. 2: Block diagram of a typical WSN.

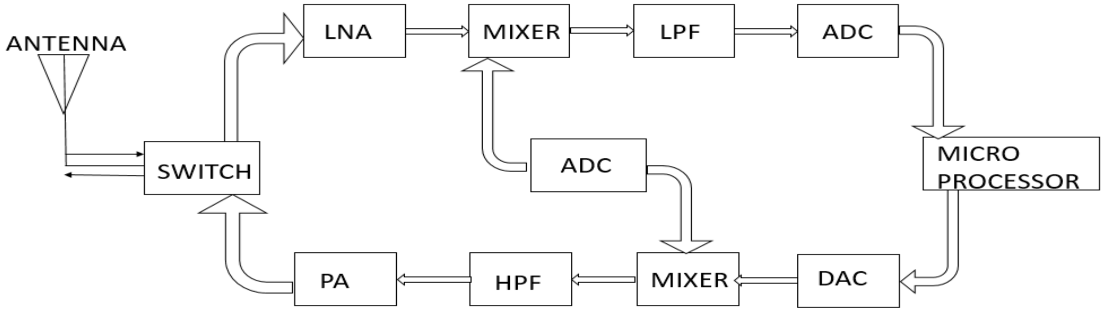


Fig. 3: Block diagram of a transmitter.

Table 1 : PA design requirement.

Parameter	**Regular**
Output Power	18dBm
PAE	30%
Stability	>1
S11	-10 dB

3. PA Design

Over the past 30 years, research on CMOS radio-frequency (RF) front-end circuits has progressed extremely quickly. The ultimate goal for the wireless industry is to minimize the trade-offs between performance and cost, and between performance and low power consumption design [8] [9][10]. The proposed Class F amplifier has low output power and good linearity based on the IEEE 802.11b communication protocol [9]. The 2.4GHz class F PA is a two stage common-source amplifier. The first stage is a driver stage, used for providing sufficient driving capability and a proper gain, as seen in figure 4(a). And the second stage is the power output stage which used for performing sufficient output power, as seen in figure 4(b)[11].

3.1. Class F PA Design

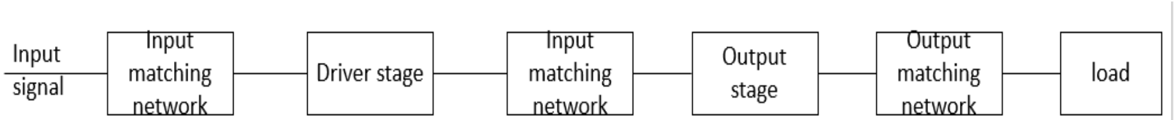
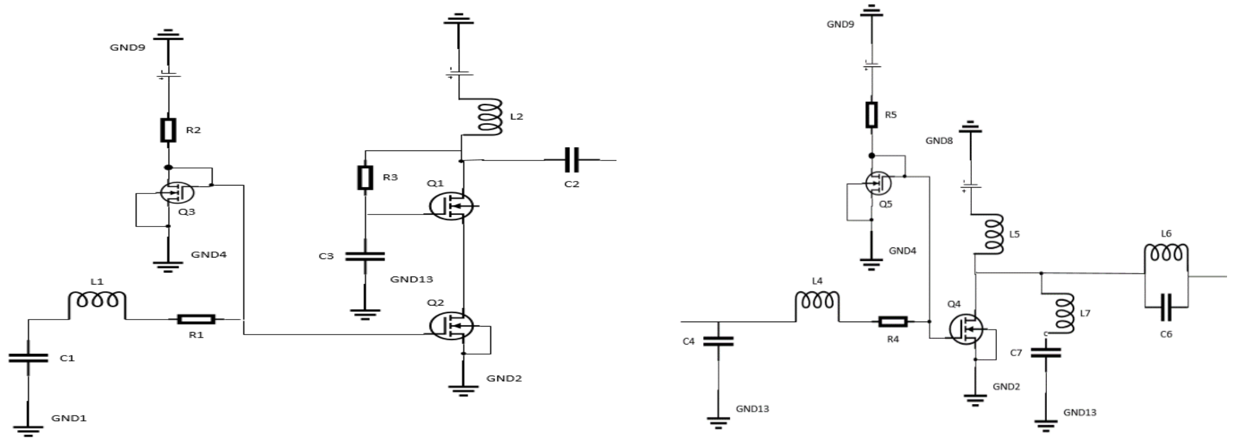


Fig. 4: Block diagram of a class F power amplifier.

Power amplifiers are critical components in daily life. One major application that touches many people’s lives is modern communication systems, such as in our cell phones. Recently, research in power amplifier technologies is becoming more and more common, due to this far-reaching impact. This research is focused on how to design power amplifiers with low power, high linearity, broadband, high power added efficiency (PAE) and low cost. In the case of Class AB power amplifiers, there is a fundamental tradeoff between linearity and efficiency [11]. For class F power amplifier, the main advantage is high performance and low power consumption. Furthermore, it has less power losses for the same frequency compare to other types of power amplifier. The class F doesn't have many components, so it makes implement in the silicon cheaper and make the cost cheaper.



(a) (b)

Fig. 5: (a) Schematic of driver stage schematic (b) Schematic of output stage schematic.

The drive stage as seen in figure 5 (a), is a cascode structure [12]. Cascode structures are a common approach to mitigate the low gain typically seen in silicon circuits. Cascode structure provide higher gain. Transistor M1 is self-biased, which reduces headroom. The component values can be seen in the Table 2.

Table 2: 2.4GHz PA driver stage component.

Parameter	**Size (Unit)**
Q1	W/L=0.6um/0.6um (f=56,m=16)
Q2	W/L=0.3um/0.6um (f=88,m=36)
Q3	W/L=0.3um/0.6um (f=2,m=6)
R1	14.5 Ohm
R2	10K Ohm
R3	80 Ohm
L1	36 nH(Q=20)
L2	15 nH (Q=20)
C1	240fF
C2	10 pF
C3	100pF

The output stage is shown in figure 5 (b). In most cases, Class F power amplifiers are usually biased as Class AB or Class B states, thus eliminating the harmonics, providing a square wave shape at the output. More specifically, the odd order harmonic impedances are infinite (besides the fundamental order), and the even order harmonic impedances are zero. So for the circuit, at the output port, the second harmonic impedance should be zero and the third harmonic impedance should be infinite. To achieve this goal, a series resonant circuit and a parallel resonant circuit are designed. In Si CMOS technology, the inductors' Q usually set as 20 for simulation. Due to its low cost, the capacitors and the inductors can be integrated on chip. But at the output stage, the inductors are large, so including them on the die has high area cost.

After the output stage and driver stage, the inter-stage matching circuit is more challenging. If the input of second stage and output of the first stage are all conjugate matched to 50Ω, the two stages can be connected directly. The complete optimized circuit is shown in Figure 6.

Table 3: 2.4GHz PA output stage component.

Parameter	**Size (Unit)**
Q4	W/L=0.3um/0.6um (f=66,m=24)
Q5	W/L=0.3um/0.6um (f=4,m=2)
R4	5 Ohm
R5	80 Ohm
L4	30 nH(Q=20)
L5	10 nH(Q=20)
L6	10 nH(Q=20)
L7	1 nH (Q=20)
C4	800 fF
C6	390 pF
C7	1.1 pF

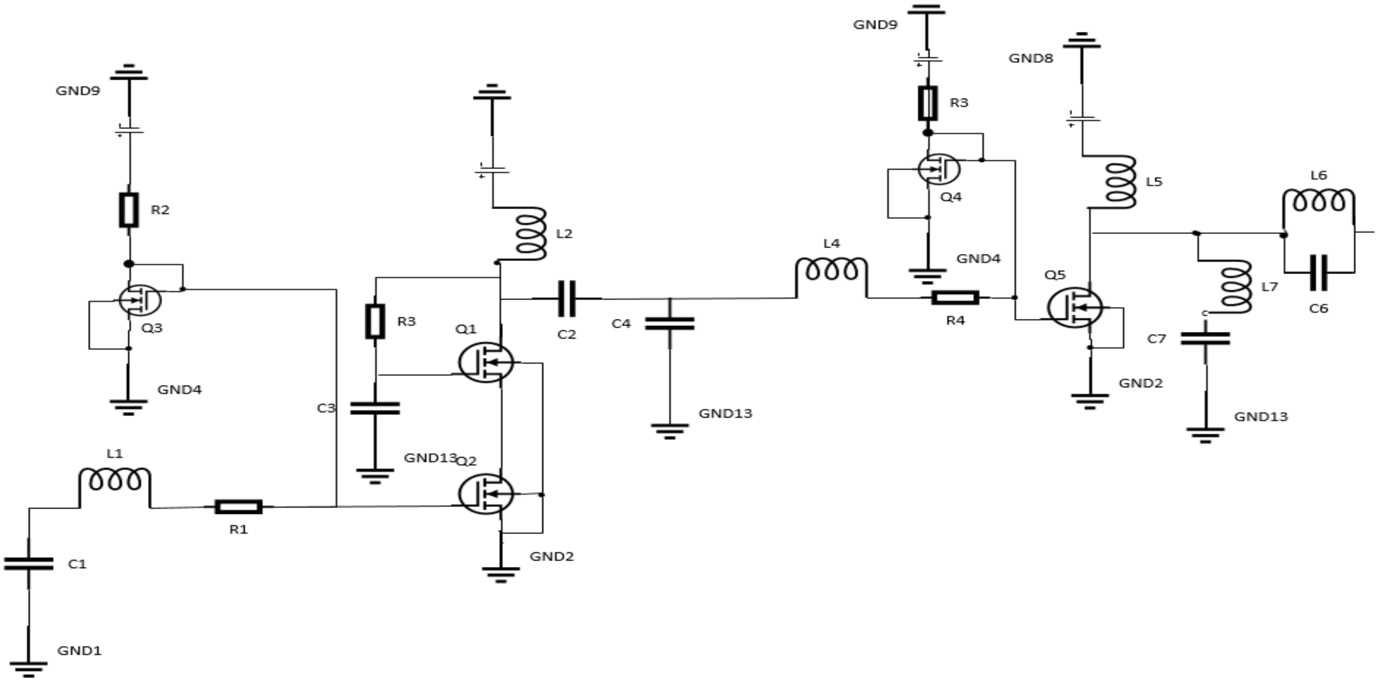


Fig. 6: Overall circuit schematic.

3.2. Results

As seen in figure 7(a), the output power is 10dBm. As seen in figure 6(b), the frequency is at 2.4 GHz the S11 is less than -10 dB, also, the total power of the PA is 3.5 W.

As seen in figure 8(a), Kf is larger than 1 for all frequencies from 1 to 3 GHz, so this circuit is totally stable. And the PAE is 46% at input power 0 dB.

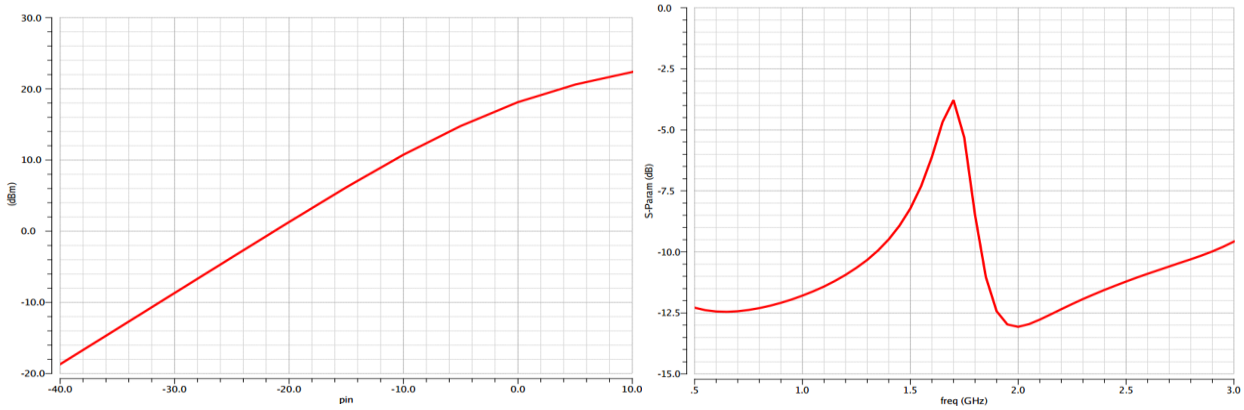
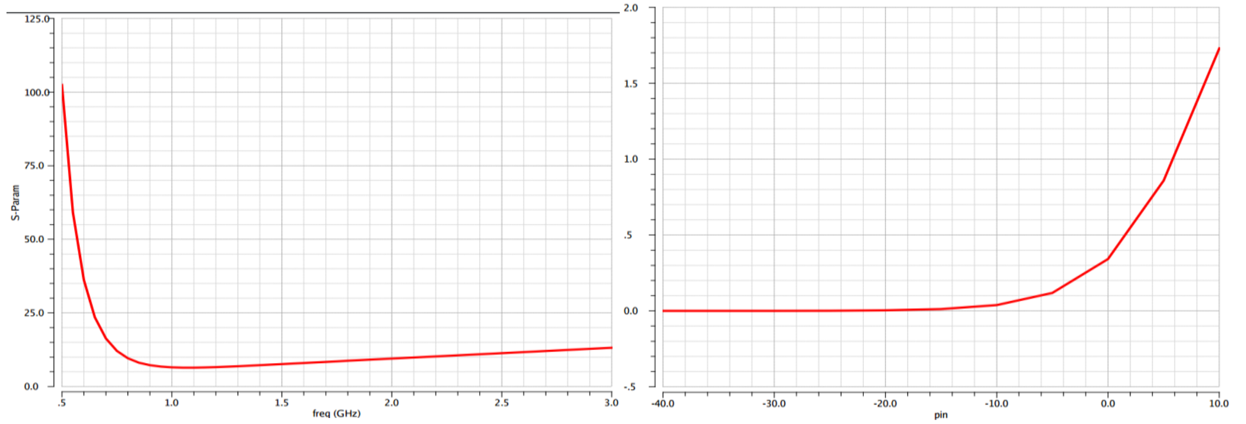


Fig. 7: (a) PA output (b) S11.



(a) (b)

Fig. 8: (a) Kf (b) PAE.

4. Conclusion

This paper describes the method of designing and simulating power amplifier using cadence software based on SIMC CMOS process 180nm technology. This PA is used for sensor networks. This research is still in the early stages of development of a low cost and low power device. In order to reach the performance that is needed, the PA process uses group III and IV elements. This circuit meets the scheduled requirements for the CMOS process, but it still has room to improve performance metrics. When the sensor is coupled with communications technologies such as mobile phones and the Internet, the sensor network constant information flow between individuals and their doctors. Such low cost and low power device can save a lot of hospitalization resources. To realize this, future improvement is needed.

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