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A Fabrication Process for Nanopatterns Shrinkage with Variable Sizes for Large Area

Shuhao Si, Lars Dittrich, Martin Hoffmann
Micromechanical Systems Group, IMN MacroNano®, Technische Universität Ilmenau
Germany
shuhao.si@tu-ilmenau.de; lars.dittrich@tu-ilmenau.de; martin.hoffmann@tu-ilmenau.de

Abstract **-** In this paper, a cost efficient process chain is designed to shrink periodic nanopatterns to tunable feature sizes. The feature size of the final patterns can be controlled and adjusted. 100 mm full wafers featuring square holes with 130 nm, 160 nm, 190 nm and 220 nm feature sizes are fabricated from the original wafer containing circular holes with a diameter of 350 nm. The fabrication chain involves well-known technologies such as etching and soft UV nanoimprint lithography (UV-NIL). Based on a single original master, an intermediate template is fabricated featuring an inversed pyramid pattern using soft UV-NIL and subsequent wet chemical etch. By utilizing the slope of the inversed pyramid structures, the mask on the final substrate can be opened featuring tunable dimensions. Cryogenic etching based on SF_6/O_2 chemistry enables the creation of the final shrunk nanopatterns with smooth and vertical profile. The fabrication cycles involve only short imprinting and etch processes coping without costly electron beam writings. Therefore, the original micro- and nanostructure wafer can be shrunk into nanopatterns with tunable feature sizes at a constant pitch in a cost effective manner. The generated periodic nanopatterns can be adopted to the fields of NIL templates, photonic crystals, optics, energy conversion and storage, etc.

Keywords**:** nanofabrication, nanopattern shrinkage, soft UV-NIL, tunable feature size, large area, low cost

1. Introduction

Device miniaturization has been in demand based on Moore's Law and the concept of "Beyond Moore's Law" 0-0. The functional structures developed from macro to micro- and nano-range. Periodic nanostructures, such as nano-pillars, cavities, line gratings, rods, and wires, have been great attractions in the field of optics, photonics, MEMS/MOEMS/NEMS, energy, life science, etc. 00. Extended patterning area enables the utilization of such nanostructures from research to industrial applications 0. Electron beam lithography (EBL), laser interference lithography (LIL) are mainly employed to produce new periodic nanopatterns. However, they are limited by the high cost and reasonable throughput when the feature size goes to e.g. sub-500 nm in large area 0.

In this paper, the feasibility of fabricating nanopatterns with tunable feature sizes in silicon at wafer-level is presented. A master wafer with periodic nanocavities directly written by EBL is used to necessarily initialize the fabrication process. An intermediate template featuring inversed pyramids is fabricated from the master wafer. Diverse nanopattern replicas with variant feature sizes can be produced utilizing the intermediate template. The fabrication processes cope with a series of soft UV nanoimprint lithography (UV-NIL) and etchings, without requiring electron beam writing. Therefore, it is accomplished at low cost and in a relatively high throughput. The feature size of the new set of nanocavities can be effortlessly tuned during the respective etch process, making it the essential motivation of this work.

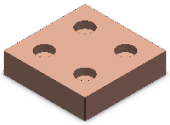
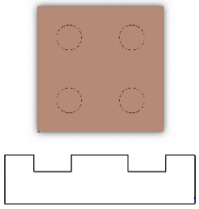
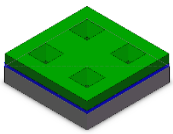
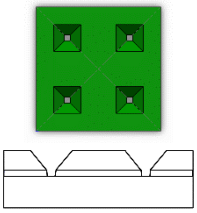
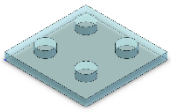
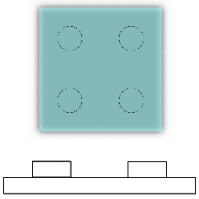
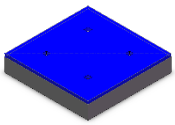
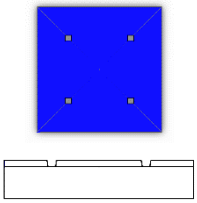
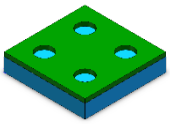
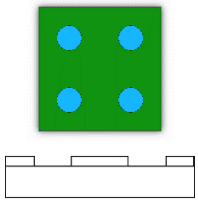
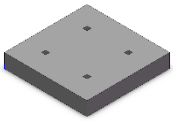
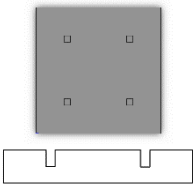
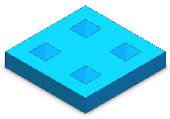
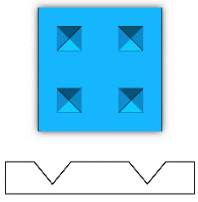
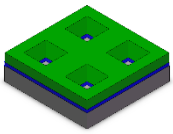
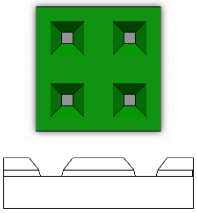
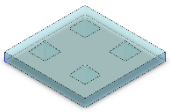
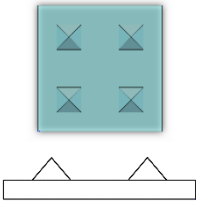
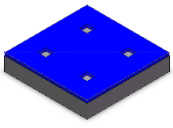
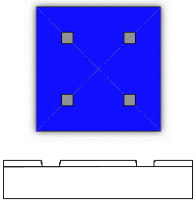
The methodology and fabrication process are explained and illustrated in the second section. Corresponding to the processing flow, the fabrication results are shown and discussed in the subsequent sections. In the last part, the potential of this methodology for the fabrication of further types of periodic nanostructures is specified. Additional applications are forecasted as well.

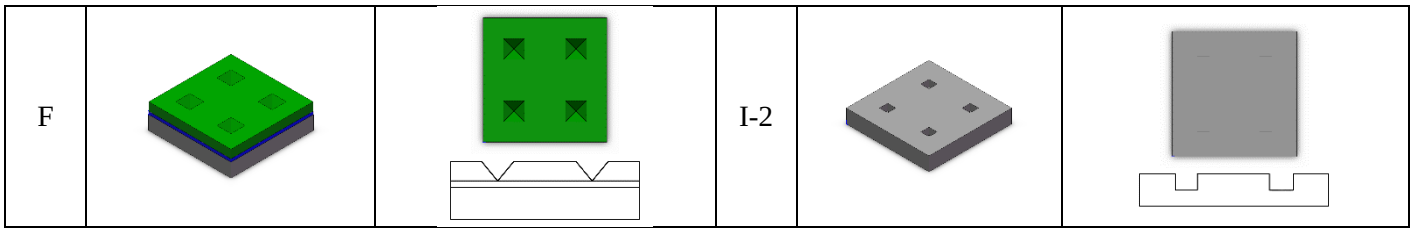
2. Methodology

The fabrication process flow to shrink the original master nanopatterns to the aspired patterns with tunable feature sizes is schematically illustrated in Table 1. A master featuring circular cavity patterns is prepared (Step *A*) by traditional nanostructure patterning technologies such as EBL and IL. Soft polymer-based stamps are replicated from the master (Step

B) to realize the large area patterning, e. g. 100 mm wafers by soft UV-NIL. The patterns are transferred from the soft stamp into the resist which is coated onto a <100>-orientated silicon substrate. A plasma etch process descums the residual resist and structures the mask on the intermediate template. Thus, the silicon substrate is masked by the identical patterns as the master (Step *C*). The intermediate template is chemically etched into inversed pyramids by means of KOH wet etching (Step *D*). The surface of the inversed pyramid intermediate template is treated with FDTS as ASL for further soft stamp replications (Step *E*). The final silicon substrate that comprises a hard mask layer on top is subsequently imprinted by the pyramid featured soft stamp (Step *F*).

Table 1: Schematic process flow of the shrinkage of nanopatterns with tunable feature sizes.

Step	3D-view	Top view (upper) and cross-section view (lower)	Step	3D-view	Top view (upper) and cross-section view (lower)
A			G-1		
B			H-1		
C			I-1		
D			G-2		
E			H-2		



The feature size of the final nanocavities is determined by the dimensions of the etch mask and is defined by the sloped sidewalls of inversed pyramids to obtain the tunable openings. A plasma etch process that is suitable for both the resist and the mask material is chosen to break through the hard mask. By applying different etch durations, the hard mask is opened with tunable sizes (Step *G-1* and *G-2*). As shown in Fig. 1, for instance, the hard mask is opened to the width of W_d by applying an etch duration *t*, resulting the height of patterned resist h_d. By increasing the etch duration, the patterned resist is etched down to the height of h_e, whereas the width of the opening is correspondingly enlarged to W_e due to the sidewall slope. Therefore, openings on the hard mask with various sizes can be controllably achieved.

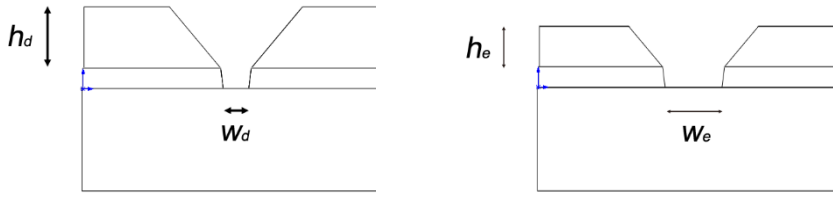


Fig. 1: Schematic diagram of the variant mask openings by different etch durations.

The residual resist can be removed after the masking (Step *H-1* and *H-2*, respectively). Considering the fact that the pyramid slope in the resist leads to non-vertical sidewalls in the hard mask after plasma etching, the hard mask ought to be preserved as much as possible for silicon substrate etching. The mask should be exposed to the plasma in a short duration to avoid long term chemical reaction and physical bombardment and it is preferably to be protected by extra passivation layers as well. Therefore, the cryogenic silicon etching is employed for the structuring of the final nanocavities. By using the masks patterned in Step *H-1* and *H-2*, respectively, the circular nanocavities from the original master are shrunk to square nanocavities with tunable feature sizes, as well as smooth and vertical sidewalls (Step *I-1* and *I-2*, respectively).

3. Results and Discussion

A UV-NIL system utilizing soft stamps (GD-N-03, Gdnano Ltd., China) has been employed for imprintings throughout this work. The system takes advantage of the bowing of the soft stamp, thus achieving the conformal contact from the center to the edge of the substrate (*center-to-edge* scheme) for up to 150 mm area in ambient atmosphere.

The master used in this work is a 150 mm silicon wafer patterned by circular nanocavities over the full wafer, featuring a diameter of 350 nm and a pitch of 500 nm (cf. Step *A*). The master is coated with FDTS at 165°C in vapor phase for one hour. The FDTS monolayer extensively reduces the surface energy of the silicon in order to enable a gentle demolding of the replicated soft stamp and the master template. Young's equation correlates the surface energy and the contact angle θ of liquid-gas interface. The contact angle of a water droplet on the FDTS-treated master surface reaches approximately 115°, which corresponds well to the literature data 00.

A hybrid bi-layer soft stamp is designed fitting in the system which is depicted in Fig.2. It consists of a 2 mm thick PDMS back carrier and a thin feature layer of approx. 150 µm toluene-diluted PDMS which carriers the patterns replicated from the master nanocavities (cf. Step *B*). It has been reported that lowering the viscosity by toluene improves the wetting behavior and hence increases the patterned height of structures 0. The fraction of toluene is kept at 20 wt%. To prepare the soft stamp, 20 wt% toluene is mixed into the PDMS which is prepared at a ratio of 10:1 (base : curing agent) beforehand and degassed thoroughly. The mixture of the toluene-diluted PDMS is spin coated on the surface of the master as feature layer and pre-baked on hotplate at 80 °C for 30 minutes. When the toluene-diluted PDMS turns to be tacky, the conventional PDMS for the back carrier is cast into a defined replication mold and co-cured with the feature layer at 80 °C for extra two hours.

The resist used in the imprinting process is mr-NIL210XP (Micro Resist Technology GmbH, Germany). It is oxygen insensitive and compatible to PDMS-based soft stamps. A 50 nm SiO_2 layer is thermally grown and serves as hard mask on a 100 mm <100>-oriented silicon wafer. After imprinting using the soft stamp, the residual resist is descummed by pure oxygen plasma. The silicon substrate is etched utilizing the patterned SiO_2 mask for a wet chemical KOH etch at a concentration of 40 % and a temperature of 80 °C. The etch rate of silicon in the KOH solution is approximate 18 nm/s whereas the etch rate of SiO_2 mask is limited to below 0.2 nm/s, which results in the selectivity larger than 90:1. The fabricated intermediate template with inversed pyramid patterns after the SiO_2 mask removed (cf. Step *D*) is shown in Fig. 3.

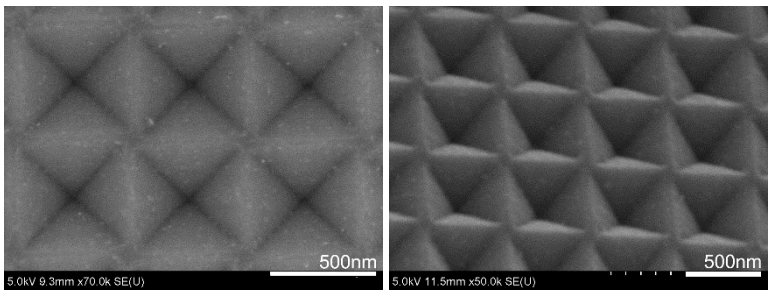


Fig. 2: SEM images of the 100 mm intermediate template with inversed pyramid patterns: top view (left) and tilted view (right).

Afterwards, the FDTS is deposited on the intermediate inversed pyramid template again to replicate the soft stamps (cf. Step *E*). 50 nm SiO_2 is thermally grown on the silicon substrate as hard mask for the subsequent etching process. Photoresist faces high risks of cracking at cryogenic temperature which is required for the final patterning and the oxygen content in the etching plasma leads to uncontrolled erosion of the mask. Therefore, an intermediate SiO_2 hard mask is preferably used to keep the fidelity of patterned surfaces. The wafer is coated with mr-NIL210XP resist for imprinting. The imprinted inversed pyramid structures in resist (cf. Step *F*) are shown in Fig. 4.

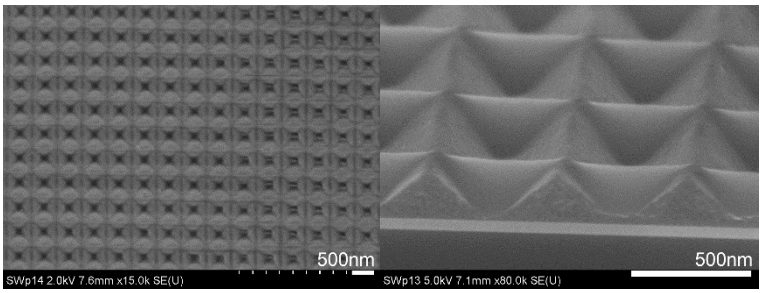


Fig. 3: SEM images of the imprinted inversed pyramid structures: top view (left) and tilted cross-section view (right).

In order to etch down both the patterned resist and open the hard mask, a reactive ion etch (RIE) process utilizing CHF_3 and Ar is used (Plasmalab 100, Oxford Instruments). The etch parameters are compiled in Table 2. As illustrated in Step *G-1* and *G-2* in Table 1, the lateral dimensions of the hard mask openings can be adjusted by applying different durations of the etch process. Fig. 5a shows that the SiO_2 mask is etched to a width of approximate 130 nm at the bottom for 2 min and 30 s. The flank angle of the mask, i.e. the angle between the sidewall and the bottom, under such etching conditions reaches nearly 80°. Fig. 5b shows that the mask opening is widened to a width of 160 nm by 2 min and 50 s break-through etch. Openings featuring a width of approximate 190 nm and 220 nm are obtained by extending the break-through etch durations to 3 min 10 s and 3 min 30 s, respectively (Fig. 5c and Fig. 5d). The residual patterned resist is stripped after the break-through etch by applying a microwave oxygen plasma (TePla 200, PVA) at 250 W for 5 min (cf. Step *H-1* and *H-2*). The microwave plasma generates a high concentration of active radicals for chemical stripping and low physical bombardment energy such that the SiO_2 mask and silicon substrate are not attacked.

Table 2: Process parameters of the break-through etch of the SiO_2 mask.

Flow rate (sccm)	RF Power (W)	Pressure (mTorr)	Temperature (°C)	Helium Backing

CHF3	Ar				
12	38	200	50	20	ON

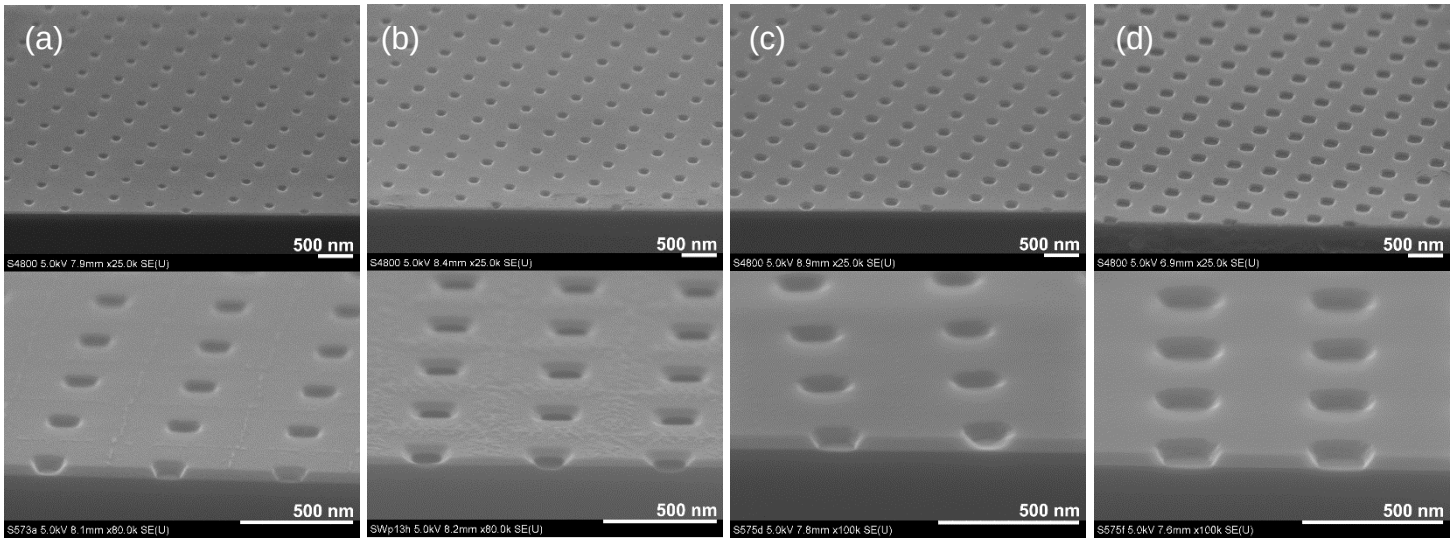


Fig. 4: SEM images of the SiO_2 mask opened to 130 (a), 160 (b), 190 (c) and 220 (d) nm on the aiming substrates.

Non-vertical sidewalls are present in the SiO_2 mask which is inevitable due to the sloping pyramid ridges in the patterned resist. The etching selectivity of SiO_2 to silicon at room temperature does not allow a silicon etching at sufficient aspect ratio without significantly consuming the mask. The consumption of mask leads to reduction of feature sizes for positive structures and expansion of feature sizes for negative structures. In order to enhance the preservation of SiO_2 mask, a cryogenic process with liquid nitrogen cooling is employed for silicon etching based on SF_6/O_2 chemistry. The cryogenic process makes use of depositing a passivation layer of silicon oxide/fluoride (SiO_xF_y) on the structure sidewalls that prevents them from fluorine radicals attacking. Additionally, the low temperature not only inhibits the radicals physically bombarding the sidewalls but also reduces the chemical consumption of the hard mask. Therefore, the energetic ions mainly penetrate the passivation layer at the bottom and rarely attack the sidewalls. In comparison to the traditional cyclic deep RIE (c-DRIE) process that involves discrete etching and passivation cycles, the cryogenic process promotes the selectivity between the silicon and SiO_2 mask without generating sidewall scallops.

An Inductively Coupled Plasma (ICP) facility (PlasmaPro 100 Cobra, Oxford Instrument) has been used throughout the etching of the final nanocavities. The ICP offers a high density of radicals without generating a large amount of kinetic energy and thus achieves a high etch rate of the silicon substrate. Studies have shown that the temperature and the amount of oxygen will delicately influence the thickness of passivation layer and, therefore, affect the profile of etched structures []. The total flow rate of SF_6 and O_2 in this case is kept at 50 sccm in which the O_2 accounts for 20 %. The bottom electrode is powered at an RF frequency of 13.56 MHz for 5 W and cooled by liquid nitrogen. The electrode temperature is maintained at -120 °C, and the substrates to be etched are placed in the process chamber for 5 min to level the temperature of substrate to the electrode. The high density plasma is generated independently by the ICP coil at a power of 500 W. The pressure is set to be 6 mTorr for the cryogenic etching. At such low pressure levels, the mean free path length of the ions is larger than the sheath thickness. Therefore, the ions will be hardly deviated from the vertical direction 00. Helium backing is provided for efficient thermal contact. The etch parameters are compiled in Table 3.

Table 3: Process parameters of the cryogenic etching of the shrunken nanopatterns.

Flow rate (sccm)		Power (W)		Pressure (mTorr)	Temperature (°C)	Helium backing
SF_6	O_2	ICP	RF			
40	10	500	5	6	-120	ON

The remaining SiO_2 mask is completely removed by hydrogen fluoride (HF) wet etch after the cryogenic structuring. The SEM images of the final shrunken nanocavities with feature dimensions of approximate 130 nm, 160 nm, 190 nm and 220 nm, respectively, are displayed in Fig. 6a to Fig. 6c. The etch rate according to the conditions in Table 3 reaches approx. 900 nm/min and the etch process lasts 15s. The cryogenic process extensively enlarges the selectivity between the SiO_2 mask and the silicon substrate. The SiO_2 mask is mostly preserved without obvious consumption and therefore the etched profile does not encounter strong expansions. The gas flow ratio of SF_6/O_2 results in a balance of the passivation layer deposition and penetration. Thus, the shrunken square nanocavities possess very smooth and vertical sidewalls, which qualifies them for applications such as NIL templates and photonic crystals.

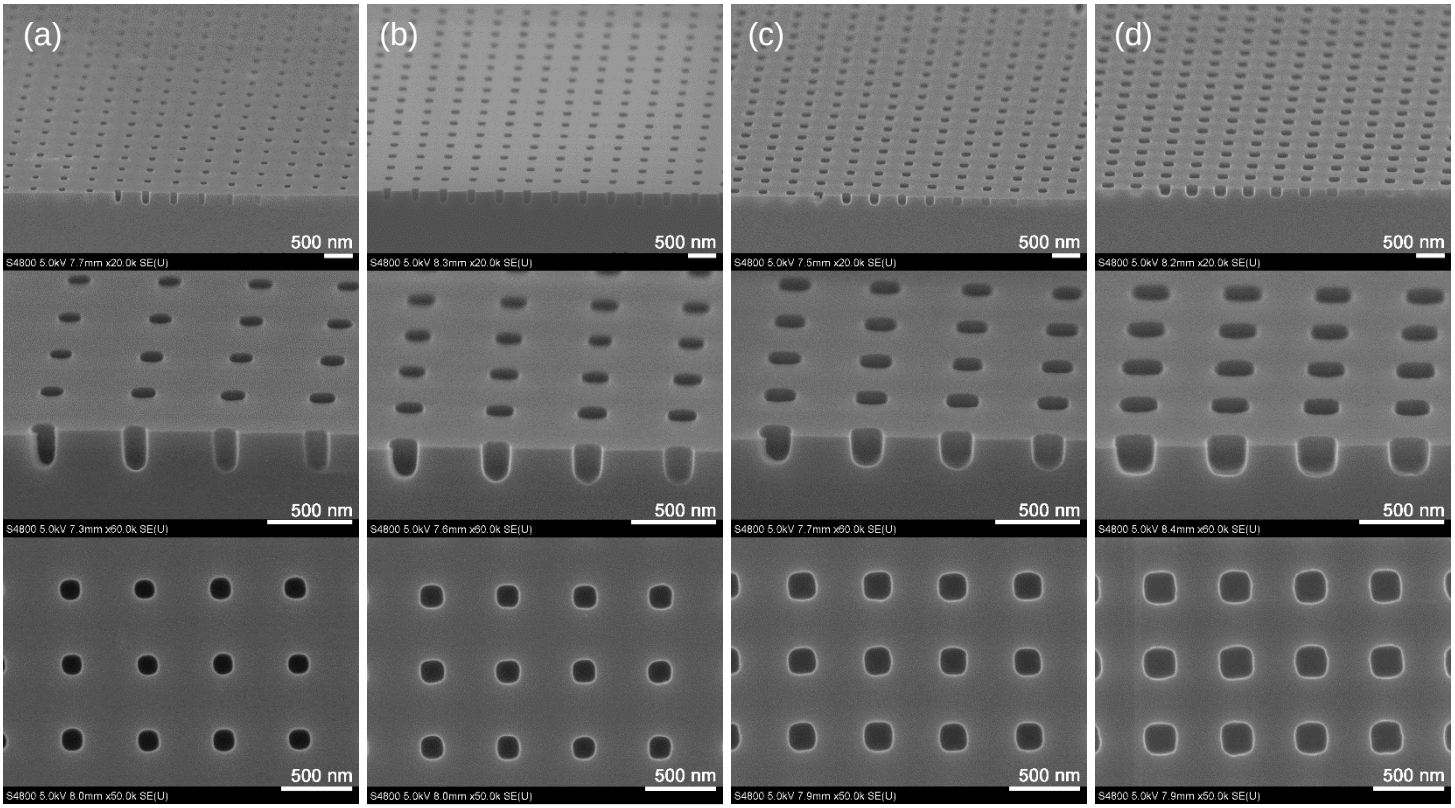


Fig. 5: SEM images of the final nanocavities with the feature size shrunk to approximate 130 (a), 160 (b), 190 (c) and 220 (d) nm.

4. Conclusion and Outlook

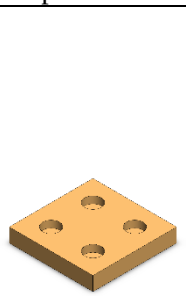
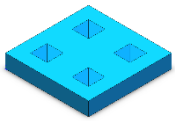
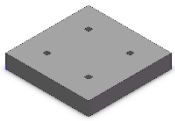
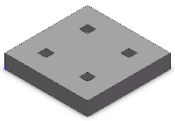
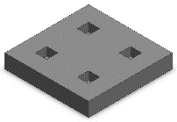
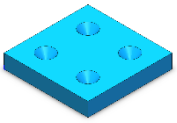
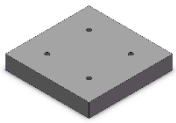
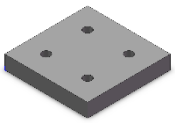
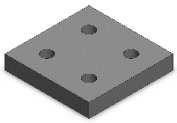
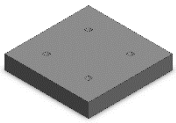
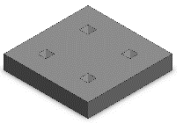
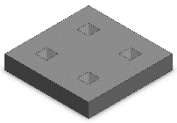
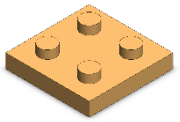
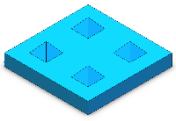
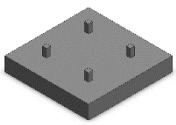
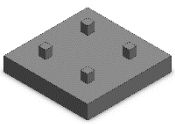
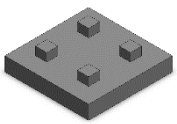
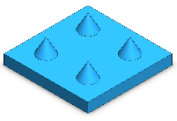
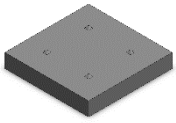
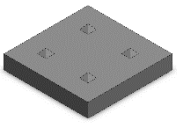
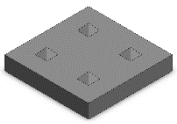
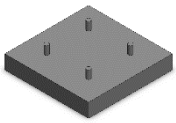
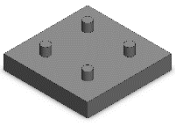
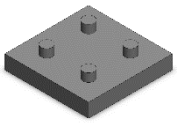
Based on a single EBL-written master wafer featuring circular nanocavities with a diameter of 350 nm, a shrinkage of nanocavities with feature size down to 130 nm, 160 nm, 190 nm and 220 nm in square layout have been fabricated in this work. The fabrication chain includes a two-stage UV-NIL and etching processes. The production cycle is kept short and simple, and therefore the cost for such fabrication is enormously reduced compared to that written by EBL and such. The introduced method provides a great cost-effective possibility to transfer the nanoscale or microscale patterns into smaller and tunable sizes whereas the pitch of the original patterns is kept constant. By delicately controlling the mask opening step, additional shrinkage of the feature size is acquirable following the same methodology and fabrication processes (Table 4A).

The most essential step in order to shrink the nanopatterns with tunable feature sizes is the fabrication of an intermediate template with sloped sidewalls. A wet chemical KOH etch is employed in the presented case to etch the <100>-oriented silicon. Square hole patterns are obtained in the final products following the topology of the pyramids. Alternatively, dry etch approaches can be utilized to fabricate inversed cone profiles instead of KOH-etched inversed pyramids (cf. Step *D*). Therefore, following the topology of the cone, the final template can be patterned with circular nanocavities with tunable feature sizes (Table 4B).

Alternatively, to etch the final template into square hole patterns by means of SF_6/O_2 cryogenic process (cf. Step *I-1* and *I-2*), the silicon substrate can be etched by KOH as well to achieve inversed pyramid nanocavities with reduced feature sizes for application-specific purposes (Table 4C).

In case a master template with positive nanostructures such as nanopillars is used, positive intermediate templates can be fabricated featuring either pyramid profile by KOH etching or cone profile by employing plasma etching. Thus, the final NIL templates can be fabricated into square pillar (Table 4D), pyramid (Table 4E) or circular pillar (Table 4F) patterns with tunable feature sizes.

Table 4: Perspectives of new nanopatterns fabrication using the shrinkage methodology.

	Master nano-patterns	intermediate template	shrunken nanopatterns with tunable feature sizes		
A					
B					
C					
D					
E					
F					
G					

By combining the metal-assisted chemical etching (MaCE) with this methodology, this method provides a great opportunity for broadening the perspectives of nanowires or high aspect ratio nanopillars (Table 4G), with porous, core/shell structures.

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